NOMURA

Global Markets Research

27 July 2026

ChangXin Memory Technologies 688825.SS 688825 CH

EQUITY: TECHNOLOGY

The DRAM in the Chinese crown; initiate at Buy

CXMT should continue to gain market share as global supply of memory could remain tight

Rating Starts at	Buy
Target price Starts at	CNY 116.00
IPO price 27 July 2026	CNY 8.66
Implied upside	+1,239.5%
Market Cap (USD mn)	

Research Analysts

Semiconductor

Donnie Teng - NIHK
donnie.teng@nomura.com
+852 2252 1439

Frank Fan - NIHK
frank.fan@nomura.com
+852 2252 2195

Asia Technology

CW Chung - NIHK
cwchung@nomura.com
+852 2252 6075

Initiate coverage at Buy with and a TP of CNY116

We initiate coverage of CXMT – China's largest DRAM maker – at Buy with a TP of CNY116. We expect CXMT's market share gain to accelerate considering that the global supply of memory is unlikely to ease in the coming years. Supported by capacity expansion, node migration, and ASP hikes, we forecast CXMT to post 63%/74% sales/net profit to parent CAGRs in 2026-28F. Our TP of CNY116 is based on 20x 2028F EPS of CNY5.8. We assign a 20x target P/E multiple as we expect CXMT to trade at 2x the valuation of its major US competitor, Micron ([MU US, Not rated]; which has traded at ~10x over the past five years), owing to market share gains and the higher valuation multiples in China's market. Downside risks include: 1) worsening of end demand; 2) intensifying competition from domestic peers such as YMTC (unlisted); 3) insufficient supply of IC and components (e.g., CPUs); and 4) escalation of geopolitical tensions between the US and China.

Demand could continue to outpace supply in the foreseeable future; CXMT appears well-positioned to gain market share

We estimate that strong demand for agentic AI will drive a more than sevenfold increase in global memory usage (with 60%+ bit CAGR) over 2026-30F, even after accounting for potential adoption of memory-efficiency technologies (discounting memory usage by 4x). However, expansion of semiconductor capacity faces multiple bottlenecks (e.g., clean rooms, equipment, materials, and talents). Memory makers are expanding capacity at a 30-40% bit CAGR over 2026-30F, but that could still be insufficient. We forecast CXMT to record bit expansion at a 40-45% CAGR over 2026-30F and its global DRAM market share to increase from ~10% currently to ~18% by end-2028F.

Impact from the MATCH Act (or potential US sanctions) is worth monitoring

The **MATCH Act** is a US export legislation designed to restrict China's access to advanced chip-making technologies by coordinating with allies to curb exports of crucial equipment and materials and preventing foreign firms from servicing machines already in China. Although CXMT may still have access to sufficient DUV domestically without using EUV to develop its upcoming 12-16nm nodes, whether it can get key foreign-made equipment (localization rate now is around 40%, according to our estimates) and materials (such as photoresist) is worth monitoring, in our view. In the worst case, we assume CXMT's capacity expansion in Shanghai (potentially 30-40% of its total capacity by 2028F) could be pushed out.

Year-end 31 Dec	FY25	FY26F		FY27F		FY28F	
Currency (CNY)	Actual	Old	New	Old	New	Old	New
Revenue (mn)	61,799	0	290,666	0	560,788	0	773,323
Reported net profit (mn)	1,875	0	130,315	0	277,248	0	393,070
Normalised net profit (mn)	1,875	0	130,315	0	277,248	0	393,070
FD normalised EPS	3.11c		2.05		4.08		5.79
FD norm. EPS growth (%)	–		6,488.6		99.0		41.8
FD normalised P/E (x)	278.0	–	4.2	–	2.1	–	1.5
EV/EBITDA (x)	5.6	–	0.2	–	-0.5	–	-0.9
Price/book (x)	9.2	–	2.3	–	1.1	–	0.6
Dividend yield (%)	–	–	–	–	–	–	–
ROE (%)	3.8		84.0		70.7		54.0
Net debt/equity (%)	169.8		net cash		net cash		net cash

Source: Company data, Nomura estimates

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See Appendix A-1 for analyst certification, important disclosures and the status of non-US analysts.

Key data on ChangXin Memory Technologies

Performance

(%)	1M	3M	12M
Absolute (CNY)			
Absolute (USD)			
Rel to CSI 300			

M cap (USDmn)	
Free float (%)	2.8
3-mth ADT (USDmn)	

Income statement (CNYmn)

Year-end 31 Dec	FY24	FY25	FY26F	FY27F	FY28F
Revenue	24,178	61,799	290,666	560,788	773,323
Cost of goods sold	-22,830	-36,465	-47,451	-60,675	-73,560
Gross profit	1,349	25,334	243,215	500,113	699,764
SG&A	-2,765	-7,319	-23,544	-42,620	-54,906
Employee share expense	-4,607	-9,593	-39,240	-72,902	-96,665
Operating profit	-6,024	8,422	180,431	384,591	548,192
EBITDA	9,780	34,778	214,438	427,598	600,199
Depreciation	-14,456	-24,680	-32,207	-41,107	-50,007
Amortisation	-1,347	-1,675	-1,800	-1,900	-2,000
EBIT	-6,024	8,422	180,431	384,591	548,192
Net interest expense	-2,204	-2,954	-2,800	-2,600	-2,400
Associates & JCEs					
Other income	-821	2,233	9,603	16,354	18,963
Earnings before tax	-9,049	7,701	187,234	398,344	564,755
Income tax	-2	-557	-13,481	-28,681	-40,662
Net profit after tax	-9,051	7,144	173,753	369,664	524,093
Minority interests	1,906	-5,269	-43,438	-92,416	-131,023
Other items					
Preferred dividends					
Normalised NPAT	-7,145	1,875	130,315	277,248	393,070
Extraordinary items					
Reported NPAT	-7,145	1,875	130,315	277,248	393,070
Dividends					
Transfer to reserves	-7,145	1,875	130,315	277,248	393,070
Valuations and ratios					
Reported P/E (x)	–	278.0	4.2	2.1	1.5
Normalised P/E (x)	-70.0	278.0	4.2	2.1	1.5
FD normalised P/E (x)	–	278.0	4.2	2.1	1.5
Dividend yield (%)	–	–	–	–	–
Price/cashflow (x)	72.5	14.3	2.5	1.5	1.0
Price/book (x)	12.6	9.2	2.3	1.1	0.6
EV/EBITDA (x)	12.6	5.6	0.2	-0.5	-0.9
EV/EBIT (x)	–	23.0	0.2	-0.5	-1.0
Gross margin (%)	5.6	41.0	83.7	89.2	90.5
EBITDA margin (%)	40.4	56.3	73.8	76.2	77.6
EBIT margin (%)	-24.9	13.6	62.1	68.6	70.9
Net margin (%)	-29.6	3.0	44.8	49.4	50.8
Effective tax rate (%)	–	7.2	7.2	7.2	7.2
Dividend payout (%)	–	0.0	0.0	0.0	0.0
ROE (%)	–	3.8	84.0	70.7	54.0
ROA (pretax %)	–	3.2	57.3	109.5	141.8
Growth (%)					
Revenue	166.1	155.6	370.3	92.9	37.9
EBITDA	-200.5	255.6	516.6	99.4	40.4
Normalised EPS	-56.7	–	6,488.6	99.0	41.8
Normalised FDEPS	-56.7	–	6,488.6	99.0	41.8

Source: Company data, Nomura estimates

Cashflow statement (CNYmn)

Year-end 31 Dec	FY24	FY25	FY26F	FY27F	FY28F
EBITDA	9,780	34,778	214,438	427,598	600,199
Change in working capital	-6,375	-38,565	-32,089	-10,873	-6,727
Other operating cashflow	3,492	40,307	37,096	-11,374	-21,154
Cashflow from operations	6,897	36,520	219,446	405,351	572,319
Capital expenditure	-71,230	-49,739	-72,000	-72,000	-72,000
Free cashflow	-64,332	-13,219	147,446	333,351	500,319
Reduction in investments	-301	-22,565	21,266	0	0
Net acquisitions					
Dec in other LT assets	2,496	247	-1,085	-1,000	-1,000
Inc in other LT liabilities	7,273	-3,624	1,100	500	500
Adjustments	-10,654	-11,142	-21,281	500	500
CF after investing acts	-65,518	-50,303	147,446	333,351	500,319
Cash dividends					
Equity issue	66,604				
Debt issue					
Convertible debt issue					
Others	76,913	45,593	0	0	
CF from financial acts	76,913	45,593	66,604	0	0
Net cashflow	11,396	-4,710	214,050	333,351	500,319
Beginning cash	31,113	42,508	37,798	251,847	585,199
Ending cash	42,508	37,798	251,847	585,199	1,085,517
Ending net debt	-4,640	96,381	-99,818	-433,170	-933,488

Balance sheet (CNYmn)

As at 31 Dec	FY24	FY25	FY26F	FY27F	FY28F
Cash & equivalents	42,508	37,798	251,847	585,199	1,085,517
Marketable securities	1	21,346	0	0	0
Accounts receivable	1,846	1,524	7,963	15,364	21,187
Inventories	18,550	28,568	32,501	38,233	42,322
Other current assets	5,110	21,750	30,000	32,000	34,000
Total current assets	68,014	110,986	322,312	670,796	1,183,026
LT investments	300	1,520	1,600	1,600	1,600
Fixed assets	153,132	183,024	222,817	253,710	275,702
Goodwill	121	123	120	120	120
Other intangible assets	48,591	39,938	33,499	27,546	22,100
Other LT assets	1,442	1,195	2,280	3,280	4,280
Total assets	271,599	336,785	582,627	957,051	1,486,829
Short-term debt	1,796	9,676	9,676	9,676	9,676
Accounts payable	6,275	8,702	11,700	14,961	19,146
Other current liabilities	49,119	34,465	18,000	19,000	20,000
Total current liabilities	57,191	52,842	39,376	43,637	48,822
Long-term debt	95,994	118,825	136,793	136,793	136,793
Convertible debt	5,194	5,678	5,560	5,560	5,560
Other LT liabilities	8,963	5,340	6,440	6,940	7,440
Total liabilities	167,342	182,685	188,169	192,930	198,615
Minority interest	62,837	97,346	140,785	233,200	364,224
Preferred stock					
Common stock	57,771	60,193	67,884	67,884	67,884
Retained earnings	-38,522	-36,650	93,665	370,912	763,982
Proposed dividends					
Other equity and reserves	22,171	33,211	92,125	92,125	92,125
Total shareholders' equity	41,420	56,754	253,673	530,921	923,991
Total equity & liabilities	271,599	336,785	582,627	957,051	1,486,829
Liquidity (x)					
Current ratio	1.19	2.10	8.19	15.37	24.23
Interest cover	-2.7	2.9	64.4	147.9	228.4
Leverage					
Net debt/EBITDA (x)	net cash	2.77	net cash	net cash	net cash
Net debt/equity (%)	net cash	169.8	net cash	net cash	net cash
Per share					
Reported EPS (CNY)	-12.37c	3.11c	2.05	4.08	5.79
Norm EPS (CNY)	-12.37c	3.11c	2.05	4.08	5.79
FD norm EPS (CNY)	-12.37c	3.11c	2.05	4.08	5.79
BVPS (CNY)	0.69	0.94	3.74	7.82	13.61
DPS (CNY)	0.00	0.00	0.00	0.00	0.00
Activity (days)					
Days receivable	27.9	10.0	6.0	7.6	8.6
Days inventory	296.6	235.8	234.9	212.8	200.4
Days payable	100.3	75.0	78.5	80.2	84.8
Cash cycle	224.1	170.8	162.4	140.2	124.2

Source: Company data, Nomura estimates

Company profile

CXMT is the largest DRAM maker in China, and the forth largest in the global market, next to Samsung, Hynix and Micron.

Valuation Methodology

Our TP CNY116 is based on 20x 2028F EPS of CNY5.8. We assign a 20x target P/E multiple as we expect CXMT to trade twice the valuation of its major US competitor, Micron, which has traded at ~10x over the past five years, due to CXMT's market share gains and the higher valuation multiples in the China market. The benchmark index is CSI300

Risks that may impede the achievement of the target price

Downside risks include: (1) worsening of end demand; (2) intensifying competition from domestic peers such as YMTC; (3) insufficient supply of IC and components such as CPUs; and (4) escalation of geopolitical tensions between the US and China.

ESG

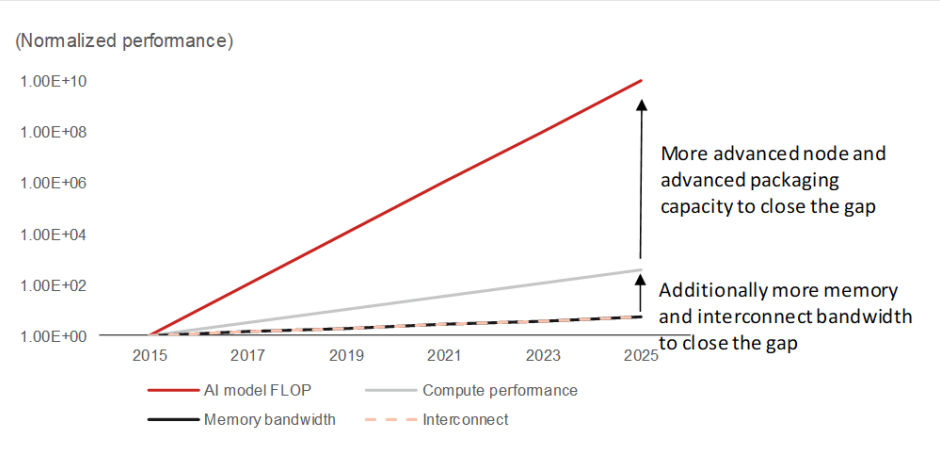
CXMT provides details of its ESG policy on the company webstie (https://www.cxmt.com/en/sustainable.html). CXMT recognizes: (1) its duty in preserving and protecting the environment and strictly follows government law and regulations; (2) it is committed to complying with all labor laws and ensuring a free, equal and fair working environment for its employees; and (3) it indicates that integrity and compliance are the basic requirements for the survival and healthy development of the company by following the highest standards of compliance and business ethics to achieve sustainable business development goals.

AI evolution could drive exponential memory demand growth

Why cloud AI and agentic AI may generate a lot of memory and networking demand

The memory industry entered a structural growth phase following the launch of ChatGPT [owned by OpenAI (unlisted)] in December 2022, which triggered considerable growth in GPU and high-bandwidth memory (HBM) demand. In modern workloads like AI and high-performance computing, memory is one of the primary performance bottlenecks as memory bandwidth cannot keep up with processor speed, where the rate of improvement in processor performance outpaces the rate of improvement in memory performance due to limited I/O and decreasing signal integrity. This disparity limits the overall system performance, as the processor spends more time waiting for data from memory, leading to a bottleneck.

Fig. 1: Performance of LLM, computer chips, memory, and interconnect



Source: Nomura research

To break through the bottleneck, the industry relies on several workarounds, including memory content and bandwidth improvement as well as higher throughput from communication networking:

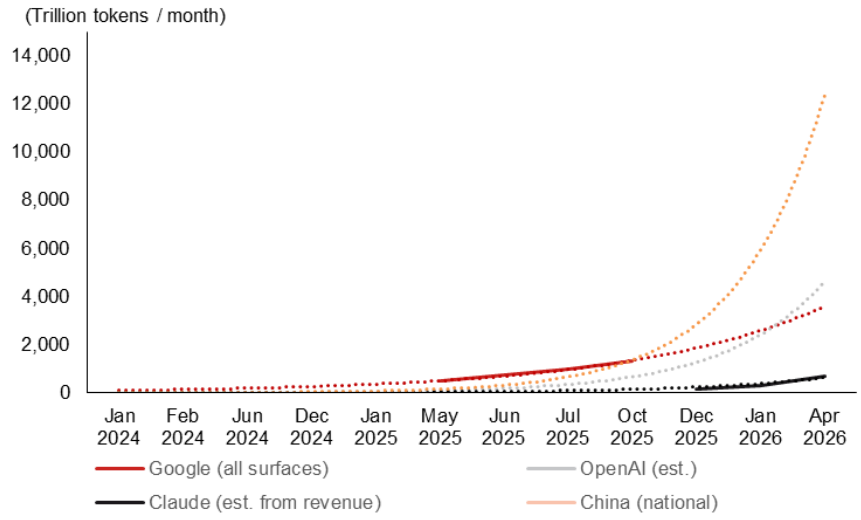
- **High bandwidth memory (HBM):** Stacking more memory chips vertically directly on the processor package to increase bandwidth and drastically reduce distance and latency.
- **Caching:** Utilizing smaller, ultra-fast on-chip memory (like SRAM) to hold frequently accessed data closer to the logic compute die.
- **Memory-on-logic or compute-in-memory:** Packaging or moving the computing logic as close as possible or directly to the memory storage area to prevent data from having to travel across the chip.
- **Compute express link (CXL):** Specialized interconnect technologies that allow processors to pool and access memory dynamically.
- **More interconnects for both copper and optical:** As copper interconnects hit physical scaling limits and traditional packages run out of die shoreline, next-generation hardware is exploring optical interconnects to separate GPUs and HBMs. This bypasses traditional physical constraints, multiplying HBM capacity and reducing electro-optical data travel times.
- **Model compression:** Reducing model size through techniques like quantization (lowering precision) or pruning to make them fit entirely into on-chip cache or HBM.

Subsequently, the adoption of retrieval-augmented generation (RAG) and agentic AI applications has accelerated demand for conventional servers and SSDs, and initiated a triple memory supercycle (commodity DRAM, HBM, and SSD) since 3Q25.

As AI semiconductor demand shifts from training toward inference workloads, memory demand is entering a period of exponential expansion. This reflects the rapid growth in KV-cache memory requirements, driven by increases in user base, user engagement time, AI task

complexity, reasoning-token consumption, and the emergence of agentic AI, where token usage per user is surging exponentially (*Fig. 2* - *3*). Memory demand effectively scales as the multiplicative function of these variables (a1 x a2 x a3 x a4 x …), implying that memory demand could rise by several thousand-fold over the next five years, in our view.

Fig. 2: Token usage trend by different LLM providers



Source: Company data, Nomura estimates

Fig. 3: Estimated token consumption by prompt cases

	Main hardware	Estimated token consumption per case							
		Simultaneous interpretation	Simple question	Structured constraint	Style expansion	RAG question	Image generation	Agent AI (report + model)	1-hour video generation
User's prompt input	CPU + DRAM	(instant translation)	"How's the weather today?"	"How's the weather toady? Please answer in 5 words or less"	"How's the weather today? Please answer like a poet."	"Explain about reasons behind national debt increase"	"Please describe today's weather in an abstract painting."	"Make earnings models and company note based on the model"	"Make a 1-hour video describing recent weather"
Scheduling	CPU + DRAM								
Input token	GPU + HBM	10	10	20	25	40	20	500	10
RAG	CPU + DRAM	-	-	-	-	5,000	-	20,000	-
Output token generation	GPU + HBM/ LPU	30	20	5	100	1,000	10,000	10,000	100,000,000
Total		40	30	25	125	6,040	10,020	30,500	100,000,010

Source: Nomura estimates

How agentic AI works and how much memory may be consumed if considering the memory efficiency technologies

When an end user asks an agentic AI to complete a task, we expect the request flows through eight distinct stages (*Fig. 4*).

Stage 1: User request arrives

The user's prompt is tokenized, batched, and queued for inference. The orchestrator parses the request and prepares an execution plan for the agentic pipeline.

Stage 2: Model weight loading

The model's parameters are loaded (or already resident) into accelerator memory. For large models, weights may be shared across multiple GPUs using tensor or pipeline parallelism.

Stage 3: Prefill/prompt processing

All input tokens are processed in parallel through the transformer layers. Attention matrices are computed and the KV cache is initialized for subsequent autoregressive decoding.

Stage 4: Reasoning and planning

The model generates a chain-of-thought plan, deciding which tools to call and in what order. Each new token extends the KV cache, and memory pressure grows with sequence length.

Stage 5: Tool execution

The agent invokes external tools such as web search, code execution sandboxes, file I/O, or API calls. This stage runs primarily on the CPU side and barely touches GPU memory.

Stage 6: Context integration

Tool results are tokenized and appended to the conversation. The model re-processes the expanded context window. The KV cache grows significantly, making this one of the most memory-intensive stages.

Stage 7: Multi-step iteration

Agentic loops repeat stages 4 through 6 multiple times. Each iteration further grows the context window. Memory pressure peaks here, potentially approaching HBM capacity limits.

Stage 8: Response generation

Final autoregressive decoding produces the output tokens. The response is detokenized, formatted, and streamed back to the user through the API gateway.

Fig. 4: Workflow and key bottlenecks of an agentic AI task

	Stage	Title	What Happens	Bottleneck	Note
	Stage 1	User Request Arrives	Tokenize → Batch → Queue (Tokenized prompt ready for inference)	CPU	(1) User prompt received via API gateway → (2) Text converted to token IDs by tokenizer → (3) Request batched with concurrent requests → (4) Orchestrator prepares agentic execution plan
	Stage 2	Model Weight Loading	Checkpoint → HBM (sharded across GPUs, weights resident in accelerator memory)	I/O	(1) Active MoE expert weights loaded to HBM (~0.51T of 4.5T params) → (2) Weights sharded across GPUs via tensor parallelism → (3) Inactive MoE experts in HBF (warm, 1.6 TB/s reload) or DDR → (4) Checkpoint files read from NVMe SSD
	Stage 3	Prefill / Prompt Processing	Parallel attention → KV cache initialized (KV cache initialized, ready for autoregressive decode)	GPU/AI ASIC	(1) All input tokens processed in parallel through transformer → (2) Attention matrices computed at every layer → (3) KV cache initialized for all prompt tokens → (4) Matrix multiplies saturate GPU register files & SRAM
	Stage 4	Reasoning & Planning	Chain-of-thought → decide tool calls (plan ready: tool calls identified with arguments)	Memory, then GPU/AI ASIC	(1) Autoregressive decode (one token at a time) → (2) Chain-of-thought reasoning; KV grows each token → (3) KV overflow: HBM → HBF (1.6 TB/s, warm) → DDR (100 GB/s, 6-12h) → SSD (24h) → (4) Tool call plan generated
	Stage 5	Tool Execution	Web search / Code sandbox / APIs (Tool results ready to integrate into context)	CPU	(1) External tools invoked on CPU side (GPU idle) → (2) Web search, code execution, RAG retrieval from NAND → (3) Results saved to DDR; general CPU servers activated → (4) Artifacts saved to NVMe SSD
	Stage 6	Context Integration	Append tool results → re-process context (context expanded, checking if more tools needed and stage 4 done)	All	(1) Tool results tokenized and appended → (2) Model re-processes expanded context → (3) KV cache grows; tiered overflow: HBM → HBF → DDR → SSD → (4) General servers activated for RAG queries
	Stage 7	Multi-Step Iteration	Cumulative repeat of Stages 4→5→6	Memory, then GPU/AI ASIC/CPU	(1) Stages 4→5→6 repeated N times → (2) KV cache at peak across all tiers: HBM + HBF + DDR + SSD → (3) General servers activated for each tool call → (4) Logging NAND accumulates with each iteration
	Stage 8	Response Generation	Decode → detokenize → stream to user	Memory, then GPU/AI ASIC	(1) Final autoregressive decoding produces output tokens → (2) Full KV cache read during each decode step → (3) Tokens converted back to text (detokenizer) → (4) Response streamed back to user via API gateway

Source: Nomura research

To complete the complicated agentic AI tasks throughout the above-mentioned eight stages of work flow, the modern AI system now heavily relies on a layered memory hierarchy, with each tier trading off speed against capacity. This results in the optimized usage of all different types of memories. We categorise and summarise the memory tiers relevant to agentic AI workloads, including the emerging high bandwidth flash (HBF) technology in *Fig. 5*. Each stage activates different memory tiers at different scales. After a complete agentic task run, we expect the peak concurrent memory consumption at stage 7 (multi-step iteration), when memory pressure is at its highest, particularly when the more complicated task requiring multiple steps of iteration repeatedly (*Fig. 6*).

Fig. 5: AI memory hierarchy

Tier	Capacity	Bandwidth	Latency	Role
Registers/Cache (SRAM)	~MB	~30+ TB/s	< 1 ns	On-chip registers and scratchpad memory inside GPU streaming multiprocessor; on-chip cache shared across compute units
HBM (DRAM)	24-192 GB	~3.3 TB/s	~100 ns	High Bandwidth Memory - stacked DRAM for weights, activations, KV cache
HBF (NAND Flash)	Up to 512 GB	~1.6 TB/s	~us	High Bandwidth Flash - 8-16x capacity of HBM (not mass production ready yet)
Host DDR (DRAM)	256 GB - 2 TB	~100 GB/s	~80 ns	System main memory for staging data and tool runtimes
NVMe SSD (NAND Flash)	TB - PB	~7-14 GB/s	~us-ms	Persistent storage for checkpoints, datasets, tool artifacts
Network	Aggregate	400-3200 Gb/s	~us	Inter-node fabric (NVLink, InfiniBand, etc.) for distributed inference

Source: Nomura research

Fig. 6: Different types of memories used in an agentic AI task work flow

HBF is not yet ready for mass production

Stage 1: User Request Arrives			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Receive	Network	API gateway routes request to inference server
2	Tokenize	DDR	Text prompt converted to token IDs via tokenizer
3	Batch	DDR	Request queued and batched with concurrent requests
4	Plan	DDR	Orchestrator prepares execution plan for agentic pipeline
→	OUTPUT: Tokenized prompt ready for inference		
Stage 2: Model Weight Loading			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Read checkpoint	SSD	Model weight files read from NVMe SSD
2	Transfer to HBM	HBM	Active MoE expert weights loaded to HBM (~0.51T active of 4.5T total at FP16 = ~1 TB)
3	Shard via NVLink	Network	Tensor parallelism distributes layers across GPUs
4	Inactive expert storage	(HBF), DDR, SSD	Inactive MoE experts in HBF (warm, 1.6 TB/s reload) or DDR5; full checkpoint on SSD (cold)
→	OUTPUT: Weights resident in accelerator memory		
Stage 3: Prefill / Prompt Processing			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Embed tokens	HBM	Input tokens looked up in embedding table
2	Compute attention	SRAM, L1/L2	Tiled attention matrices computed on-chip per layer
3	Init KV cache	HBM	K and V tensors stored for all prompt tokens (~300 KB/token weighted avg across model sizes)
4	FFN forward pass	SRAM, HBM	Feed-forward layers process all tokens in parallel
→	OUTPUT: KV cache initialized, ready for autoregressive decode		
Stage 4: Reasoning & Planning			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Decode token	SRAM	One new token generated via matmul in registers
2	Attend to KV	L1/L2, HBM	Attention computed over full KV cache (grows each step)
3	Extend KV cache	HBM, (HBF), DDR, SSD	New K,V appended each token. Overflow path: HBM → HBF (warm, 1.6 TB/s) → DDR5 (6–12h) → SSD (24h)
4	Generate plan	HBM	Chain-of-thought tokens identify tools to call
→	OUTPUT: Plan ready: tool calls identified with arguments		
Stage 5: Tool Execution			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Parse tool calls	DDR	Model output parsed to identify tool name + arguments
2	Execute tools	DDR, SSD, Network	GPU IDLE. Tools run on CPU. RAG reads from SSD (vector DB). General CPU servers activated
3	Receive results	DDR, Network	Tool responses from backend CPU servers. Each tool call activates 20–50 backend servers (search, DB, RAG)
4	Save artifacts	SSD	Downloaded files, code output saved to NVMe
→	OUTPUT: Tool results ready to integrate into context		
Stage 6: Context Integration			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Tokenize results	DDR	Tool output text converted to tokens
2	Append to context	HBM	New tokens added to conversation context
3	Re-process attention	SRAM, L1/L2, HBM	Model re-processes expanded context (similar to prefill). Compute-bound if many new tokens added
4	Extend KV cache	HBM, (HBF), DDR, SSD	KV grows significantly with tool results. Overflow: HBM → HBF (warm) → DDR5 (6–12h reuse) → SSD (24h cold)
→	OUTPUT: Context expanded — more tools needed? → Stage 4 | Done? → Stage 8		
Stage 7: Multi-Step Iteration			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Check completion	DDR	Orchestrator checks if more tool calls needed
2	Loop back to S4	HBM, (HBF), DDR, SSD	Stages 4→5→6 repeat. KV cache grows across all tiers with each iteration
3	KV cache at peak	HBM, (HBF), DDR, SSD	PEAK per-request memory. Hot KV in HBM, warm in HBF (1.6 TB/s), reusable in DDR5 (6–12h), cold in SSD (24h)
4	Accumulate state	DDR, SSD, Network	Tool states, history buffers, checkpoints saved
→	OUTPUT: Task complete — all tools called, results integrated		
Stage 8: Response Generation			
Step	**Action**	**Memory Tiers Active**	**What Happens**
1	Final decode	SRAM, L1/L2	Autoregressive token generation.
2	Read full KV	HBM	Full KV cache read from HBM each decode step. After completion, KV begins tier transition lifecycle
3	Detokenize	DDR	Token IDs converted back to text string
4	Stream response	Network	Response tokens streamed to user via API in real-time
→	OUTPUT: ☑ Response delivered to user		

Source: Nomura research

We note that three different layers of memories will be consumed in the eight stages of running the agentic AI tasks, including per task used memory (mainly SRAM, HBM and DDR, used for end user-specific KV cache), shared memory (mainly HBM, DDR, and SSD for model weights, checkpoint, and KV reuse pool), and persistent storage (mainly SSD and HDD for cold data storage once the data are generated as well as RAG and KV cold pool). For the memory demand trend in the future driven by agentic AI, there are two major variables that may impact the demand trend, including:

1. **The concurrent agentic AI task numbers per year (+):** This includes the number of AI users, the agentic AI adoption rate, the agentic AI tasks per annum globally, the average duration time of an agentic AI task.
2. **The memory usage discount driven by memory efficiency technologies (-):** This includes KV quantization, GOA (grouped query attention), PagedAttention, prompt/prefix caching, MLA (multi-head latent), TurboQuant, etc.

Several memory-efficiency technologies could dramatically reduce the memory footprint of AI inference. Critically, these techniques stack multiplicatively – combining attention architecture compression with KV cache quantization and memory management yields compound reductions of 4-40x. However, the practical memory savings is unlikely to exceed 5x, as weight KV quantization, converting weights and activations of running LLMs and neural networks from high-precision data types such as 32-bit floating points (FP32) or 16-bit floating points (FP16) into lower-precision integers such as 8-bit (INT8) or 4-bit (INT4), is the single-largest factor, in our view, while KV compression adds on top but is smaller than weight adjustments.

We estimate that the demand for concurrent agentic AI will drive task numbers per year to grow strongly during 2026-30F, i.e., increase 50x higher by 2030F vs 2026F, although with the memory usage discount driven by memory-efficiency technologies, which would still drive the memory usage for agentic AI tasks by more than 10x. In a scenario in which the demand for non-AI applications does not grow, AI applications could still drive a memory demand CAGR of more than 60% over 2026-30F (growing by more than 7x), on our assumptions. Key risksinclude: agentic AI usage and adoption rate by end-users falling short of our expectations; and memory-efficiency technologies driving more memory savings than we currently forecast.

Fig. 7: Major memory efficiency technologies

Memory Efficiency Technologies	Reduction	Target	Details
FP8/INT4 KV Quantization	2-4×	KV bit-width	Halves cache memory with minimal accuracy impact. Natively supported in vLLM.
GQA (Grouped Query)	8×	KV heads	Llama 3: 8 KV heads for 64 query heads. Near-zero quality loss.
PagedAttention	2-4×	KV waste elimination	Reduces allocation waste from 60–80% to <4%. Default in vLLM, SGLang, TensorRT-LLM.
Prompt / Prefix Caching	2-10x	Repeated prefixes	Reuses KV state of shared prompts. Anthropic: 90% cost reduction. 31% of queries share similarity.
MLA (Multi-Head Latent)	~15×	KV representation	DeepSeek: projects K/V into learned low-dimensional latent space.
TurboQuant	5-6×	KV bit-width (3-bit)	Google: PolarQuant + QJL. Near Shannon-optimal. 100% NIAH recall at 104K tokens.

Source: Company data, Nomura research

Fig. 8: Memory usage in different stages of agentic AI work flow

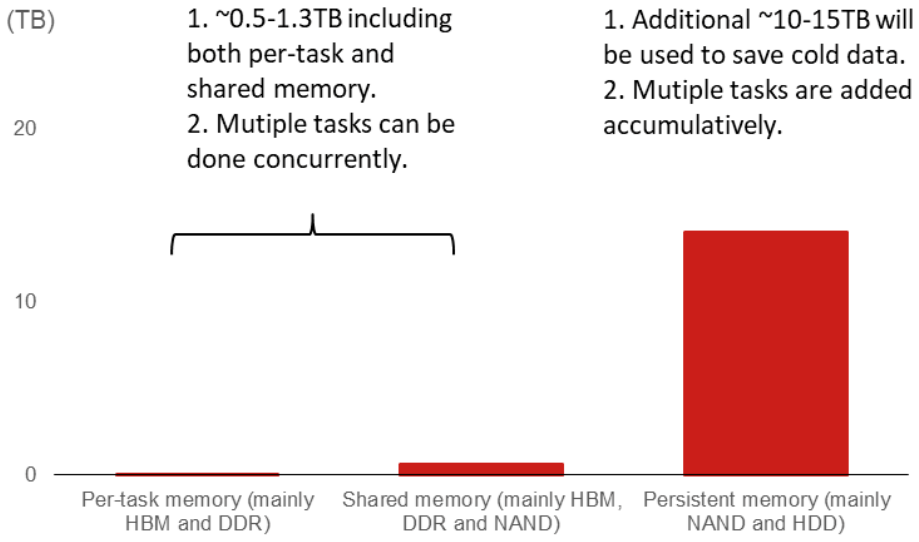
This includes the per-task and shared memory used in the different stages, but not the cold storage for data saving.

Stage	Title	Peak Memory Usage (Baseline)	Peak Memory Usage (Optimized)	Reduction	Efficiency Techniques Applied	How Efficiency Techniques to Save Memory Usage
Stage 1	User Request Arrives	~10 MB	~10 MB	1×	N/A	Nothing — this stage is CPU-side only
Stage 2	Model Weight Loading	~1–5 TB (shared by concurrent tasks)	~0.25–1.25 TB (shared by concurrent tasks)	~4×	INT4 weight quantization	INT4: active weights 1TB→250GB; checkpoint 4TB→1TB. Both 4× from quantization.
Stage 3	Prefill / Prompt Processing	~0.5–1.0 TB (shared by concurrent tasks)	~0.25–0.5 TB (shared by concurrent tasks)	~2×	INT4 weights + GQA + PagedAttention + FP8 KV	Weights 4× smaller (INT4). KV init small relative to weights. Net ~2× because weights dominate.
Stage 4	Reasoning & Planning	~0.5–1.3 TB (shared by concurrent tasks)	~0.25–0.3 TB (shared by concurrent tasks)	~2–4×	MLA (7×) + TurboQuant (5×) = up to 35× KV compression	KV cache 10-35× smaller (MLA+TurboQuant). Weights 4× (INT4). Net ~2-4× because weights dominate DRAM.
Stage 5	Tool Execution	~1–5 GB	~1–5 GB	1×	N/A	Nothing — this stage runs on CPU (DRAM/SSD/network)
Stage 6	Context Integration	~0.5–1.1 TB (shared by concurrent tasks)	~0.25–0.3 TB (shared by concurrent tasks)	~2–4×	MLA + TurboQuant + PagedAttention	Expanded KV compressed 10-14×. Weights 4×. HBF/SSD overflow reduced proportionally. Net ~2-4×.
Stage 7	Multi-Step Iteration	~1.5–5.3 TB (shared by concurrent tasks)	~0.5–1.3 TB (shared by concurrent tasks)	~3–4×	All stacked: MLA × TurboQuant × PagedAttn × FP8	PEAK: weights 4× (INT4), KV 10-12× (MLA+TurboQ), checkpoint 4× (INT4). Net ~3-4× total.
Stage 8	Response Generation	~0.5–1.1 TB (shared by concurrent tasks)	~0.25–0.3 TB (shared by concurrent tasks)	~2–4×	INT4 weights + GQA + FP8 KV	Weights 4× smaller; final KV cache reads compressed
TOTAL	All Stages (Peak Memory Usage)	~1.5–5.3 TB (shared by concurrent tasks)	~0.5–1.3 TB (shared by concurrent tasks)	~3–4×	MLA + TurboQuant + INT4 + PagedAttn + Caching	*Weight quantization (4×) is the largest single factor. KV compression (10-35×) adds on top but KV is smaller than weights. Jevons Paradox: savings consumed by longer contexts and more users.*

Source: Nomura estimates

Fig. 9: Average memory usage per task can be done concurrently within a year

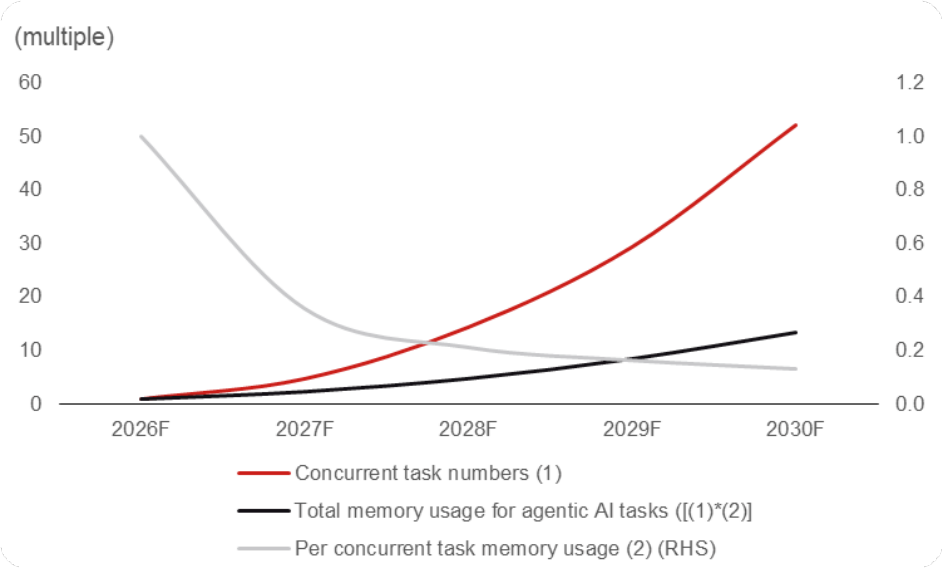
Multiple tasks can be done concurrently through different users who can share the memory pool, but the cold data from all the different users need to be stored accumulatively.



Source: Nomura estimates

Fig. 10: Memory usage for agentic AI tasks in 2026-30F

As concurrent agentic AI task numbers could grow meaningfully,
this may overcome the impact of memory efficiency technologies and drive strong memory demand.



Source: Nomura estimates

AI demand could potentially grow if AI bots run tasks themselves

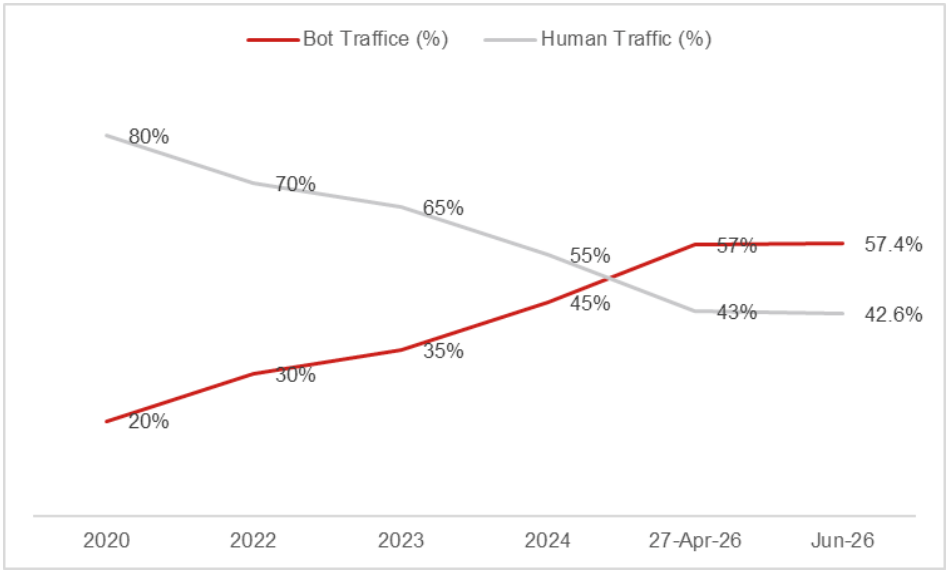
According to the Cloudfare CEO's comment (*news link*), the rapid increase in agentic internet traffic has implied that "bots have now passed human traffic online for the first time in the Internet's history". Hence, we raise the qualitative question **"what if the AI bots can run tasks themselves without the constraint by human beings"**? In this case, the demand upside could be much bigger, as the constraint only depends on:

1. **Whether human beings authorized AI bots to do so (security concern);**
2. **The limitation of infrastructure including utility, semiconductor chips, data centers, etc., and most importantly, talents;**
3. **Capex limitations of capex cloud companies, enterprises and end-users.**

In the most extreme case, in our view, we may need to seriously consider that the demand potentiality of agentic AI could be enormous, while in the coming years, semi capacity expansion is facing its biggest bottleneck – the shortfall in clean rooms, equipment, materials, and most importantly, humans.

Fig. 11: Bots vs human web traffic

Bots now generate more web traffic than humans.

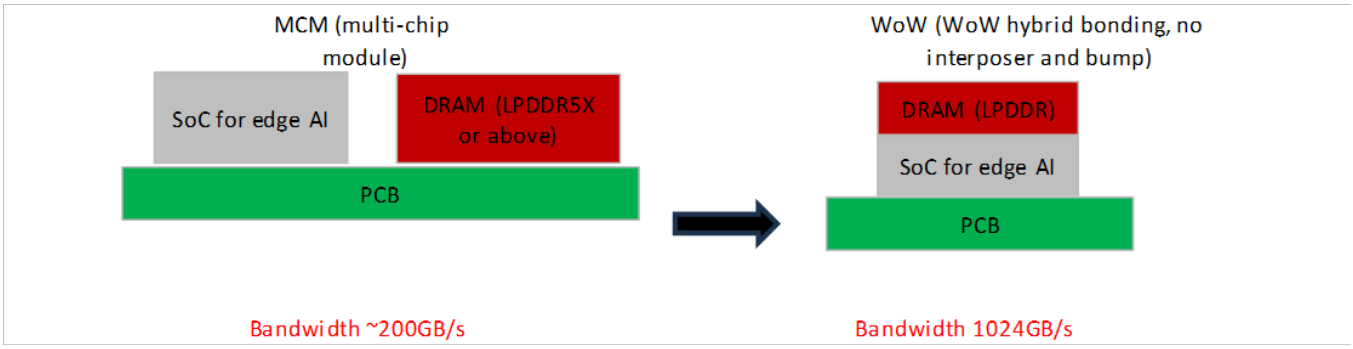


Source: Cloudfare

DRAM-on-logic wafer-on-wafer (WoW) stacking an emerging trend that could grow meaningfully in late 2027F

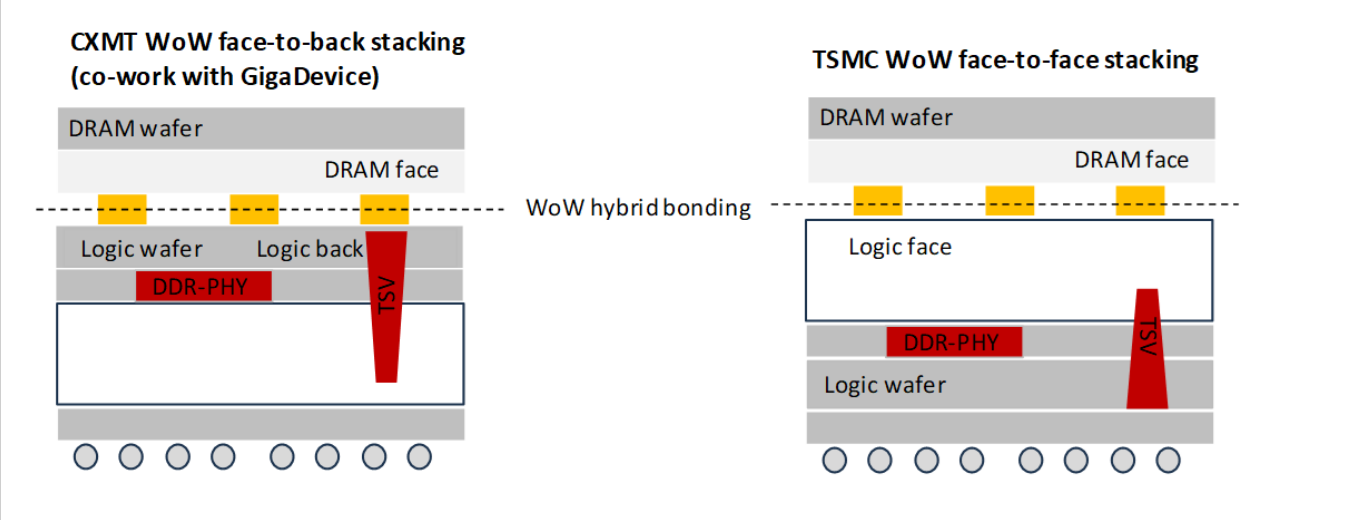
AI inference is a memory-bound task in the smart-edge domain requiring high memory bandwidth and energy efficiency with modest compute power in between 45 and 100+TOPS. Based on our assumptions, the DRAM-on-logic WoW can achieve 1TB/s bandwidth for throughput higher than 100 TPS (tokens per second). We believe this technology could gain strong momentum from late 2027F, led by AI agents in the automotive smart cockpit, premium smartphone/PCs, and robotics segments. CXMT and GigaDevice co-work on the DRAM-on-logic production and design to address the rising demand for edge AI/physical AI in China, as China is one of the largest markets that is likely to replicate its successful experience on expanding the consumer AIoT market into the physical AI market, driven by the increasing amount of smart car, robotics, Clawbot, and industry/medical applications.

Fig. 12: Difference between MCM vs WoW for edge AI chips



Source: Nomura research

Fig. 13: Different types of WoW stacking



Source: Company data, Nomura research

Fig. 14: Key WoW projects in 2026-28F in China

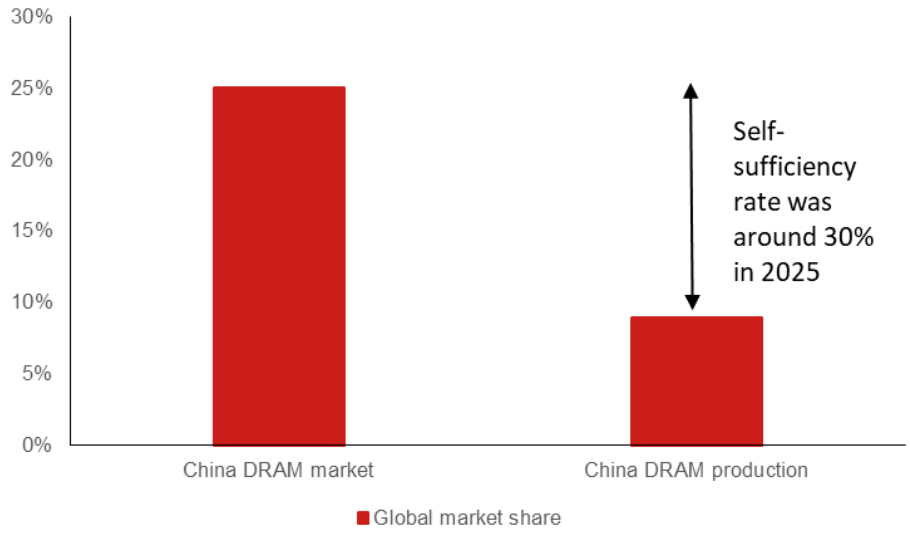
2026	2027	2028
X-Ring (for EV)	Bitdeer (NPU for server)	X-Ring (for SP)
QCOM (for SP)	Bytedance (for server)	UniSoC (for SP)
Rockchip (AIoT)	DJI (for AIoT)	Amlogic (for Clawbot)
Tanscputing (AI PC)	Rockchip (for Clawbot)	Allwinner (for Clawbot)

Source: Nomura research, Nomura research

China's DRAM production self-sufficiency rate remains low

According to WSTS, China accounted for ~25% of global DRAM market in 2025. However, according to our estimates, the market share of Chinese domestic DRAM makers (including CXMT and other domestic players) in terms of production revenue was only ~10% of the global DRAM market. Thus, the self-sufficiency rate of DRAM production by domestic players was only around 30% in 2025, which implies the domestic DRAM makers such as CXMT still have meaningful room to grow market share in China.

Fig. 15: China's DRAM market share vs domestic China's DRAM production market share in 2025



Source: WSTS, Nomura research

Memory supply growth is likely lower than demand growth due to physical constraints

We assume a memory demand CAGR of 60% over 2026-30F; in contrast, we expect an industry supply CAGR of around 30-40%; thus whether the undersupply can realistically be resolved is worth monitoring, in our view.

At present, the industry is striving to narrow this widening supply-demand gap through multiple software- and architecture-level optimizations, as we have noted in the section on memory efficiency technologies. However, we believe these solutions merely slow the pace of growth rather than reversing the trend. Therefore, every available approach – including NAND offloading (which offers over 100x higher capacity despite slower speeds) and the adoption of ultra-high-bandwidth NAND (HBF) – will likely need to be deployed simultaneously, in our view. But this may also cause the NAND supply to be even tighter and may not be able to help relieve the already tight DRAM supply effectively.

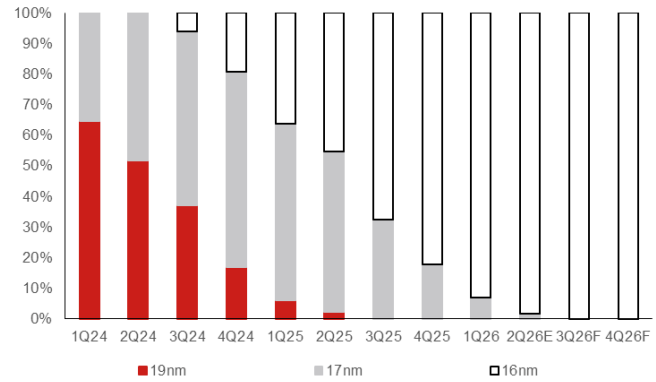
What are CXMT's technology capabilities and pricing?

We estimate CXMT's current mainstream technology in 2026F is around the 1x-1y node (around 16-17nm), with the yield rate of its DDR5 product at around 80% and DDR4 at 90%+. The company is likely pushing forward the technology to 1z-1a node (around 10-15nm) with HBM3 mass production capability from 2027F onwards.

For 15nm and 10nm node development, we expect CXMT to continue pushing the technology migration forward without using EUV. However, the photoresist supply for sub-12nm node could be a concern, as the high-end photoresist is now mostly supplied by Japan-based companies. For HBM, we believe CXMT has sent HBM3 samples to the leading ICT company and other companies in China, but qualification could take time. On the other hand, HBM3e technology is under development.

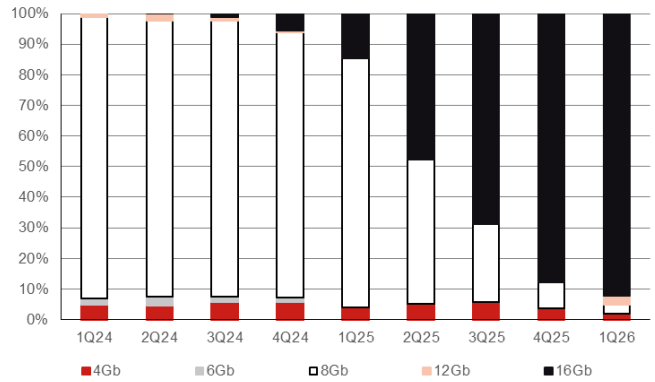
When it comes to pricing, our channel checks with some of the leading domestic smartphone and PC/server OEM companies indicate that CXMT's pricing is lower than that of the leading overseas DRAM companies, but not significantly. We estimate the pricing is around **0-20% lower, primarily due to Beijing's policy to support local tech companies that can procure memories with a more favorable price**. However, considering that CXMT's mainstream technology lags the leading overseas DRAM companies' by around five years, we estimate its gross die per wafer could be only a few hundred dies vs more than one thousand dies for the leading overseas DRAM companies. Hence, we estimate CXMT's 2026F wafer ASP at around USD14-15k. However, we expect CXMT's bit growth per wafer to improve further in 2027-28F due to its node migration from 16-17nm to 14-15nm, thereby increasing the ASP further to USD21-25k (*Fig. 16* - *18*).

Fig. 16: CXMT – shipment breakdown by technology node



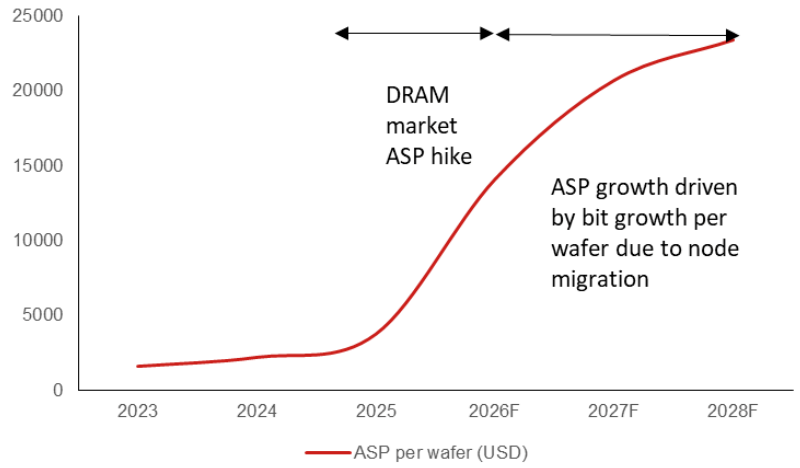
Source: DRAMexchange, Nomura research

Fig. 17: CXMT: shipment breakdown by density



Source: DRAMexchange, Nomura research

Fig. 18: CXMT's wafer pricing trend



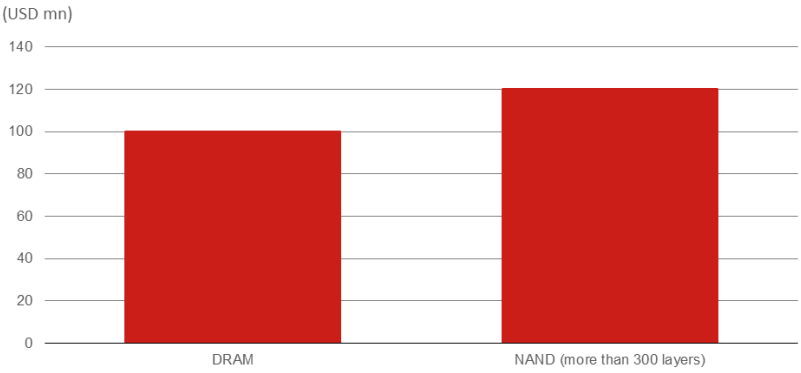
Source: Company data, Nomura estimates

How much capacity can CXMT expand by 2028F?

CXMT plans to actively develop and launch next-generation products (beyond LPDDR5X/DDR5, such as HBM3 production) to serve future customer demand. The company raised CNY57.9bn (approximately USD8.55bn) via IPO on the Shanghai Stock Exchange's STAR Market on 27 July. Once an over-allotment (green shoe) option is exercised, the maximum fund raised will climb to CNY66.6bn (USD9.83bn). It costs around USD100mn for every 1kwpm capacity expansion for DRAM (*Fig. 19*), and we estimate CXMT had 280kwpm of capacity in Heifei and Beijing as of end-2025, and will increase to 350kwpm by end-2026F. It is likely to add an additional 100kwpm capacity each in 2027F and 2028F, which would make its total capacity to reach 550kwpm by end-2028F. On the other hand, CXMT is also building up HBM packaging capacity in Shanghai (Xingpu Tianying) potentially with 50kwpm of packaging capacity with room for further DRAM production capacity expansion (*Fig. 20*).

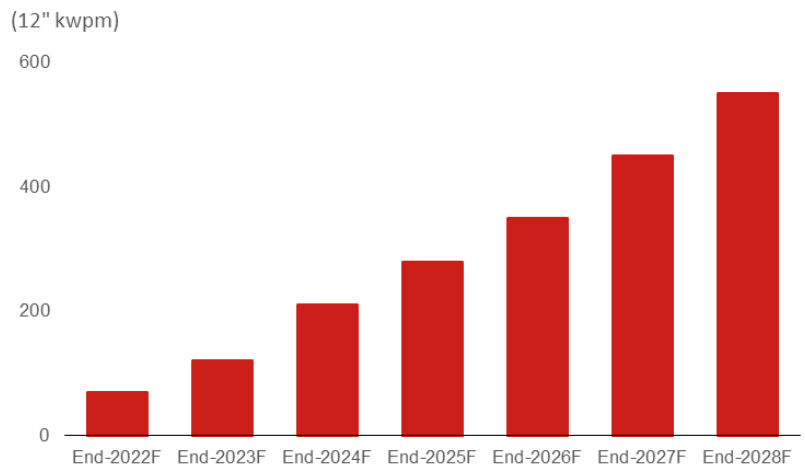
Based on our capacity forecasts, and assuming CXMT runs its fabs at full capacity utilization in 2026-30F, the wafer shipment CAGR over 2026-30F would be around 20-25%. Assuming CXMT upgrades its technology node every two years, the bit growth CAGR would be around 40-45%. Although CXMT's bit CAGR is higher than the industry average of 30-40%, it could still be below the market demand CAGR of over 60%. That said, we expect CXMT to continue to gain market share from its global peers (*Fig. 21*).

Fig. 19: Capex requirement for 1kwpm capacity expansion



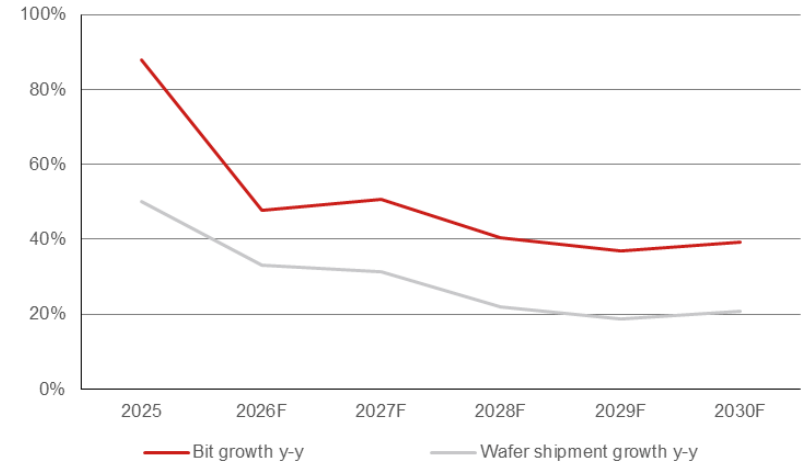
Source: Nomura estimates

Fig. 20: CXMT capacity trend



Source: Nomura estimates

Fig. 21: CXMT: bit growth and wafer shipment growth



Source: Nomura estimates, DRAMexchange

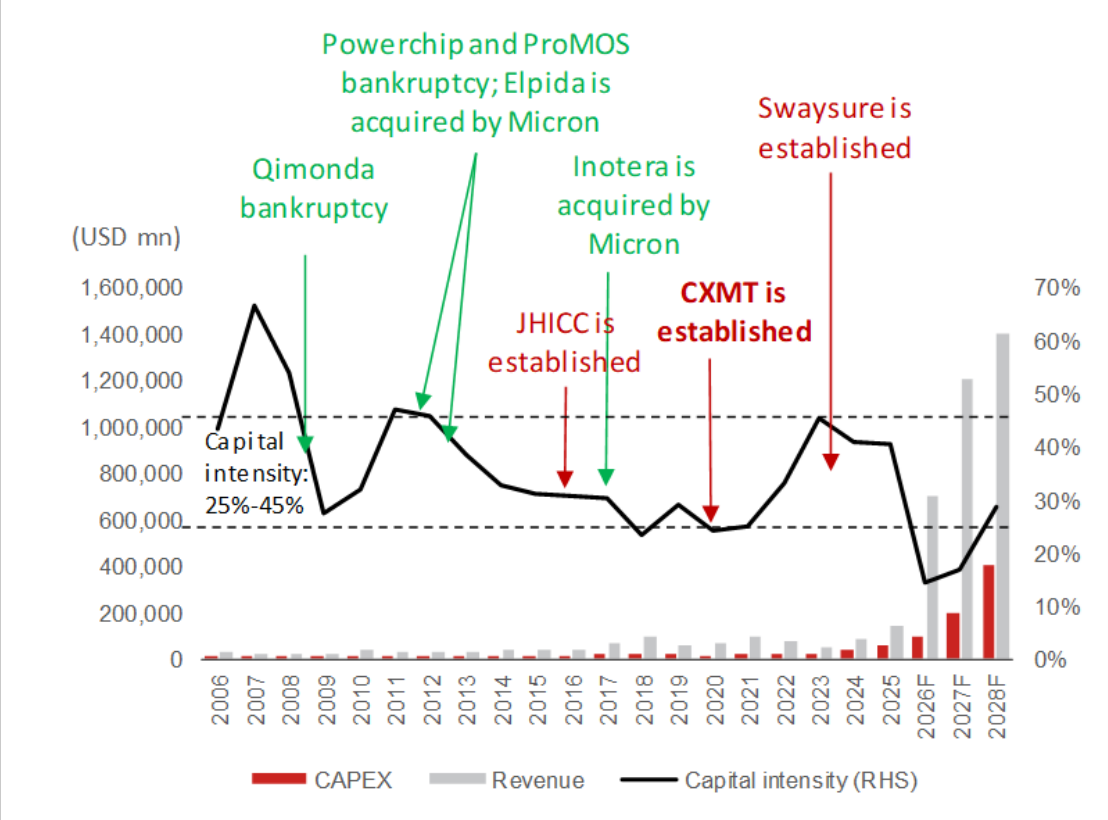
Global DRAM supply/demand dynamics remain favorable as demand is too strong but capex spending is lagging behind

In general, we acknowledge market concerns around the risk of a sharp DRAM market correction precipitated by unmanageable capacity expansion, considering the cyclical nature of the industry. However, historically, DRAM companies' capital intensity (capex-to-sales ratio) has remained mostly in the 25-45% range over the past 15 years. However, in view of the strong AI-driven memory demand since Sep-2025, capital intensity may drop significantly to only 15% in 2026F (*Fig. 22*). This implies that the DRAM market is likely to be able to absorb a much higher capex across the DRAM makers, which includes domestic DRAM companies such as CXMT.

However, as memory prices have gone up significantly since Sep-2025, we expect memory companies and their customers to gradually understand that it would be healthier for memory prices to stabilize in the coming quarters. Indeed, we have seen long-term memory supply agreements (LTAs) being reached between memory companies and their key customers. Thus, from 2028F onwards, we think memory companies will focus more on reasonable capacity expansion to drive sales and steadily improved earnings rather than pushing for memory prices to significantly grow from current levels. We also expect memory companies to meet varied customer demands rather than solely AI demand in order to maintain healthy supply/demand dynamics (*Fig. 23*).

Fig. 22: Historical DRAM capex to market (dollar amount) ratio

The capital intensity of DRAM production is currently too low due to the much bigger DRAM market



Source:WSTS, Gartner, DRAMexchange, Nomura estimates

Fig. 23: DRAM supply demand outlook

Total DRAM supply and demand	2022	2023	2024	2025	2026F	2027F	2028F	2029F	2030F
Production (mn GB)	29,333	28,954	33,400	41,098	52,901	62,756	75,478	98,299	128,385
y-y	**26%**	**-1%**	**15%**	**23%**	**29%**	**19%**	**20%**	**30%**	**31%**
Wafer capa year-average (k/wpm)	1,655	1,652	1,725	1,976	2,178	2,278	2,545	2,972	3,491
Wafer output year-average (k/wpm)	1,639	1,414	1,602	1,927	2,190	2,380	2,598	3,031	3,557
Utilization	99%	86%	93%	98%	101%	104%	102%	102%	102%
Wafer output y-y	9%	-14%	13%	20%	14%	9%	9%	17%	17%
Bit/wafer y-y	15%	14%	2%	2%	13%	9%	10%	12%	11%
Shipment (mn GB)	24,707	27,990	32,939	42,576	54,738	67,844	83,580	102,681	125,988
y-y	**2%**	**13%**	**18%**	**29%**	**29%**	**24%**	**23%**	**23%**	**23%**
Inventory (mn GB)	5,688	6,652	7,112	5,635	3,797	-1,291	-9,393	-13,776	-11,379
Inventory weeks	12.0	12.4	11.2	6.9	3.6	-1.0	-5.8	-7.0	-4.7
Price (USD/GB)	3.2	1.9	3.2	4.0	13.7	18.6	17.9	17.2	16.3
y-y	**-19%**	**-41%**	**66%**	**26%**	**245%**	**36%**	**-4%**	**-4%**	**-5%**
Revenue (mn USD)	79,978	53,175	103,824	168,738	747,421	1,260,946	1,496,746	1,766,044	2,059,762
y-y	**-17%**	**-34%**	**95%**	**63%**	**343%**	**69%**	**19%**	**18%**	**17%**

Commodity DRAM supply and demand	2022	2023	2024	2025	2026F	2027F	2028F	2029F	2030F
Production (mn GB)	29,273	28,582	31,859	37,921	48,045	55,692	65,050	83,115	106,278
y-y	**25%**	**-2%**	**11%**	**19%**	**27%**	**16%**	**17%**	**28%**	**28%**
Wafer capa year-average (k/wpm)	1,595	1,589	1,544	1,659	1,756	1,703	1,780	1,978	2,199
Wafer output year-average (k/wpm)	1,591	1,351	1,420	1,625	1,791	1,805	1,833	2,037	2,265
Utilization	100%	85%	92%	98%	102%	106%	103%	103%	103%
Wafer output y-y	9%	-15%	5%	14%	10%	1%	2%	11%	11%
Bit/wafer y-y	15%	15%	6%	4%	15%	15%	15%	15%	15%
Shipment (mn GB)	24,649	27,628	31,417	39,828	50,514	60,617	72,740	87,288	104,746
y-y	**2%**	**12%**	**14%**	**27%**	**27%**	**20%**	**20%**	**20%**	**20%**
Inventory (mn GB)	5,676	6,629	7,072	5,165	2,695	-2,229	-9,920	-14,093	-12,561
Inventory weeks	12.0	12.5	11.7	6.7	2.8	-1.9	-7.1	-8.4	-6.2
Price (USD/GB)	3.2	1.8	2.7	3.4	13.8	18.0	17.0	16.0	15.0
y-y	**-20%**	**-43%**	**50%**	**24%**	**305%**	**31%**	**-6%**	**-6%**	**-6%**
Revenue (mn USD)	78,878	50,234	85,930	135,351	694,816	1,091,101	1,236,581	1,396,609	1,571,185
y-y	**-18%**	**-36%**	**71%**	**58%**	**413%**	**57%**	**13%**	**13%**	**13%**

HBM DRAM supply and demand	2022	2023	2024	2025	2026F	2027F	2028F	2029F	2030F
Production (mn GB)	60	372	1,541	3,177	4,856	7,064	10,428	15,184	22,107
y-y	**33%**	**520%**	**314%**	**106%**	**53%**	**45%**	**48%**	**46%**	**46%**
Wafer capa year-average (k/wpm)	60	63	181	318	423	575	765	994	1,292
Wafer output year-average (k/wpm)	48	63	181	302	399	575	765	994	1,292
Utilization	80%	100%	100%	95%	95%	100%	100%	100%	100%
Wafer output y-y	7%	32%	187%	66%	32%	44%	33%	30%	30%
Bit/wafer y-y	25%	30%	44%	24%	15%	1%	11%	12%	12%
Shipment (mn GB)	58	362	1,522	2,748	4,225	7,227	10,840	15,393	21,242
y-y	**16%**	**527%**	**320%**	**80%**	**54%**	**71%**	**50%**	**42%**	**38%**
Inventory (mn GB)	12	22	41	470	1,102	939	527	317	1,182
Inventory weeks	11.0	3.2	1.4	8.9	13.6	6.8	2.5	1.1	2.9
Price (USD/GB)	19.0	8.1	11.8	12.2	12.5	23.5	24.0	24.0	23.0
y-y	**90%**	**-57%**	**45%**	**3%**	**2%**	**89%**	**2%**	**0%**	**-4%**
Revenue (mn USD)	1,100	2,941	17,894	33,386	52,605	169,845	260,165	369,434	488,577
y-y	**120%**	**167%**	**508%**	**87%**	**58%**	**223%**	**53%**	**42%**	**32%**
HBM bit mix	0.2%	1.3%	4.6%	6.5%	7.7%	10.7%	13.0%	15.0%	16.9%
HBM revenue mix	1%	6%	17%	20%	7%	13%	17%	21%	24%
HBM wafer mix	2.9%	4.5%	11.3%	15.7%	18.2%	24.2%	29.4%	32.8%	36.3%

Source: Company data, Nomura estimates

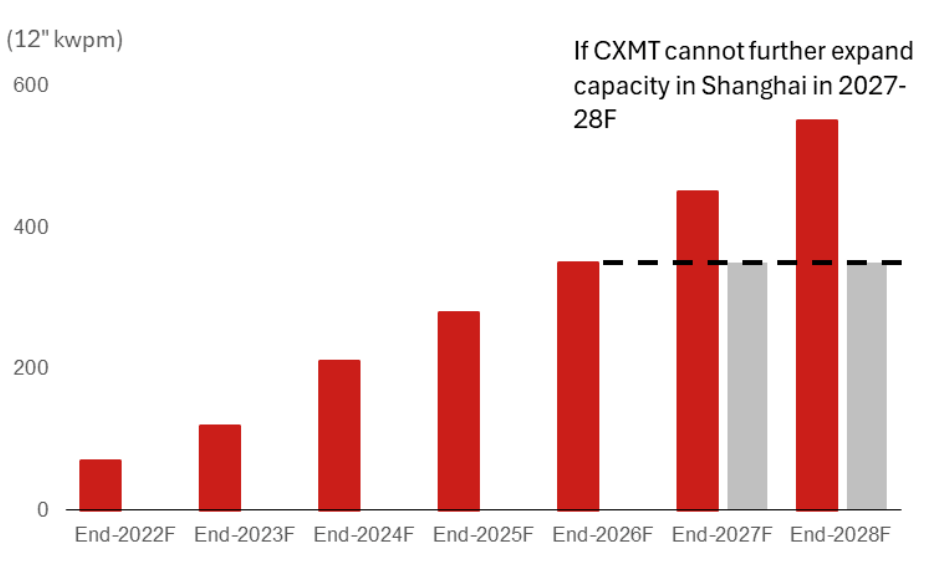
Key risk to CXMT: MATCH Act (or potential US sanctions) is worth monitoring

The MATCH Act, or any type of US sanction such as the Entity List, could be a potential downside risk to our investment thesis for CXMT. Although CXMT may continue to have access to sufficient DUV domestically without using EUV to develop its upcoming 12-16nm nodes, whether it can get key foreign-made equipment and materials is worth monitoring, in our view.

Based on our assumptions, we estimate CXMT's current domestic equipment localization rate is around 40%. If CXMT were to be prohibited from importing foreign-made equipment and forced to increase its localization rate urgently, it would likely negatively impact CXMT's production yield rate. On the other hand, for materials such as photoresist, currently most of the high-end products are dominated by Japan-based companies such as TOK (4186 JP, Neutral), JSR (unlisted), and Shin-etsu (4063 JP, Neutral) without any substitution in China. If CXMT were to be prohibited from importing Japan-made photoresist, it might be unable to further migrate its production node to sub-15nm.

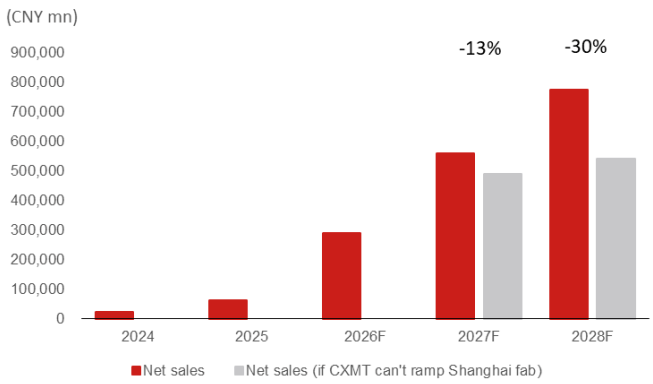
Consequently, in the worst case scenario, we assume CXMT's capacity expansion in Shanghai (which is linked with the company's advanced node (sub-15nm) and HBM production), could be pushed out. Potentially, there could be two DRAM production phases in Shanghai (100kwpm per phase), along with HBM packaging capacity of 50kwpm. If the 200kwpm capacity in 2027F/28F were removed, we expect CXMT's revenue and net profit to the parent company would be down by 13%/30% and 14%/33%, respectively.

Fig. 24: CXMT: Capacity trend, with and without the Shanghai fab



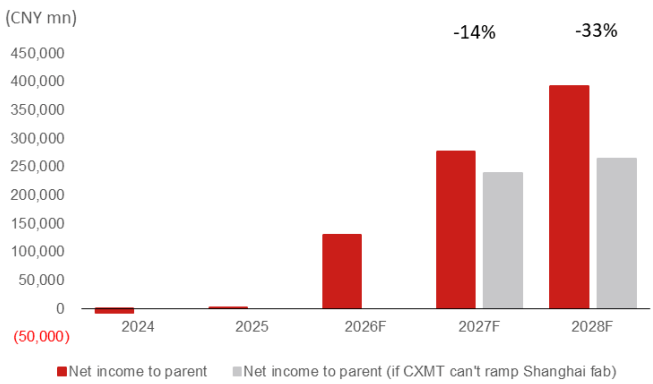
Source: Nomura estimates

Fig. 25: CXMT: Sales trend, with and without the Shanghai fab



Source: Company data, Nomura estimates

Fig. 26: CXMT: Net profit trend, with and without the Shanghai fab



Source: Company data, Nomura estimates

Key domestic equipment, material, and OSAT partners

According to CXMT's prospectus and our research, owing to CXMT not being on the US's Entity List, we estimate its current domestic equipment localization rate remains less than 40%, and will evaluate the domestic suppliers carefully by considering different aspects, including the impact on production yield rate and profitability. Below are some key domestic equipment, material and OSAT partners of CXMT.

Equipment

Etching: AMEC (688012 CH, rating suspended) and Naura (002371 CH, rating suspended) are key domestic suppliers, while AMEC has superior performance, particularly on high-aspect ratio etching.

ALD: Leadmircro (688147 CH)

Wafer bonding: Piotech (688072 CH, Not rated) and Wisdom (unlisted) are potential suppliers, while Piotech has more superior performance.

Inspection: Jingce (300567 CH, Not rated) and Skyverse (688361 CH, Not rated)

Cleaning: ACM Research (ACMR US, suspended)

Stripper: Mattson Technology (BEST, 688729 CH, Not rated)

C-SAM/SAT for back-end package: SBT (688392 CH, Not rated)

Material

Semi wafer: Eswin (688783 CH, Not rated) and NSIG (688126 CH, Neutral)

Chemicals: Yoke (002409 CH, Not rated) and Konfoong (300666 CH, Not rated)

Gas: G-Gas (688548 CH, Not rated)

CMP pad/slurry: Dinglong (300054 CH, Buy) and Anji (688019 CH, Buy)

OSAT partners

DRAM: Payton (under 000021 CH, Not rated), Xinfeng (unlisted), JCET (600584 CH, Buy), TFME (002156 CH, Buy), and TSHT (002185 CH, Buy)

HBM: Xinpu Tianying (CXMT in-house, Not rated), Xinfeng, JCET and TFME.

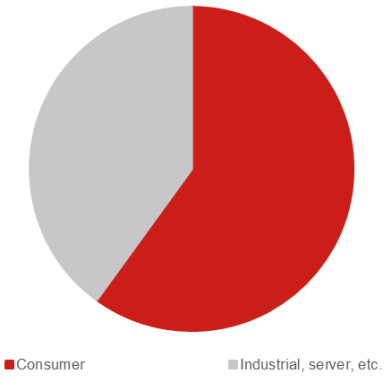
Major customers and revenue breakdown of CXMT

CXMT sells primarily through a distributor-led model (85%+ of revenue via distributors, remainder direct sales). Top-5 customer concentration: 74.12% (2023), 67.30% (2024), and 68.08% (2025) of the company's main business revenue.

Named end-customers include: Alibaba Cloud, ByteDance, Tencent, Lenovo, Xiaomi, Transsion, Honor, OPPO, and vivo. The company also notes that GigaDevice Group (controlled by Chairman Zhu Yiming) is a customer.

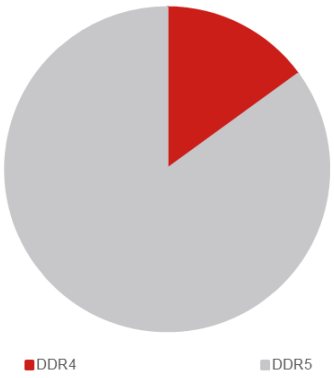
Revenue is split by product: The LPDDR series accounted for 66.43% of 2025 revenue (up from 74.54% in 2023), while the DDR series contributed 31.87% (up from 20.16%), reflecting the ramp-up in DDR5 server products. For HBM, we expect CXMT has sent HBM3 samples to the leading ICT company and other companies in China, but qualification could take time. On the other hand, HBM3e technology is under development.

Fig. 27: CXMT: revenue breakdown by end applications in 2026F



Source: Nomura estimates

Fig. 28: CXMT: capacity breakdown by different specs of DDR in 2026F



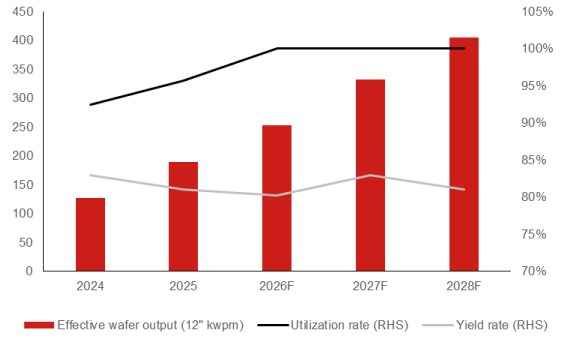
Source: Nomura estimates

Earnings forecast

We estimate CXMT had 280kwpm capacity by end-2025, and will increase to 350kwpm by end-2026F. CXMT is likely to add additional 100kwpm each in 2027F and 2028F, which would take its total capacity to 550kwpm by end-2028F. On the other hand, CXMT is also planning to build HBM packaging capacity in Shanghai (Xingpu Tianying), with 50kwpm capacity potentially (packaging only rather than DRAM production). As we expect CXMT to run at full capacity over the coming two years, we believe the key variable for wafer output should be mainly yield rate. We expect CXMT's yield rate could be volatile in between 75-85% depending on its technology migration progress and product mix (e.g., DDR5 has a lower yield rate than DDR4, and HBM production initially may carry a lower yield rate).

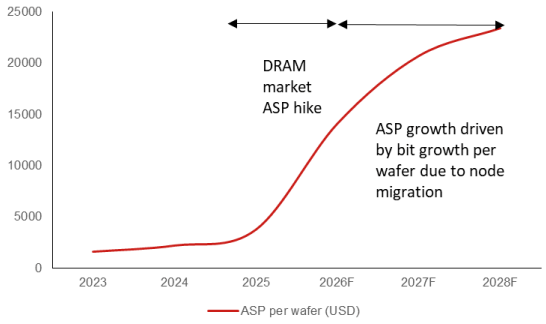
As CXMT's mainstream technology has lagged the leading overseas DRAM companies by around five years, its gross die per wafer, on our assumptions, could be only a few hundred dies vs the leading overseas DRAM companies of over 1,000 dies. Thus, we estimate CXMT's wafer ASP at around USD14-15k in 2026F. However, we expect CXMT's bit growth per wafer will improve in 2027-28F due to its node migration from 16-17nm to 14-15nm. Thus, we forecast ASP will increase further to USD21-25k. Hence, we estimate that CXMT's sales will grow 35-400% in 2026-28F with net profit to the parent company growing 40-6,000% over the same period.

Fig. 29: CXMT: capacity and utilization rate



Source: Company data, Nomura estimates

Fig. 30: CXMT: wafer price



Source: Company data, Nomura estimates

Fig. 31: CXMT: P&L

(CNY mn)	2024	2025	2026F	2027F	2028F
Net sales	24,178	61,799	290,666	560,788	773,323
COGS	22,830	36,465	47,451	60,675	73,560
Gross profit	**1,349**	**25,334**	**243,215**	**500,113**	**699,764**
SG&A and others	5,710	8,020	16,721	28,846	38,323
R&D expenses	4,607	9,593	39,240	72,902	96,665
Op income	**(8,969)**	**7,721**	**187,254**	**398,364**	**564,775**
Net non-op income	**(80)**	**(20)**	**(20)**	**(20)**	**(20)**
Pretax income	(9,049)	7,701	187,234	398,344	564,755
Tax expenses	2	557	13,481	28,681	40,662
Net income	**(9,051)**	**7,144**	**173,753**	**369,664**	**524,093**
Net income to parent	**(7,145)**	**1,875**	**130,315**	**277,248**	**393,070**
EPS (CNY)	**-0.1**	**0.0**	**2.1**	**4.1**	**5.8**

Profitability (%)	2024	2025	2026F	2027F	2028F
Gross margin	5.6	41.0	83.7	89.2	90.5
Op margin	-37.1	12.5	64.4	71.0	73.0
PBT margin	-37.4	12.5	64.4	71.0	73.0
Net margin	-29.6	3.0	44.8	49.4	50.8

YoY (%)	2024	2025	2026F	2027F	2028F
Sales		156	370	93	38
Gross profit		1,778	860	106	40
Op incomue		N/A	2,325	113	42
Net income		N/A	2,332	113	42
Net income to parent		N/A	6,851	113	42
EPS		N/A	6,741	99	42

Source: Company data, Nomura estimates

Valuation and risks

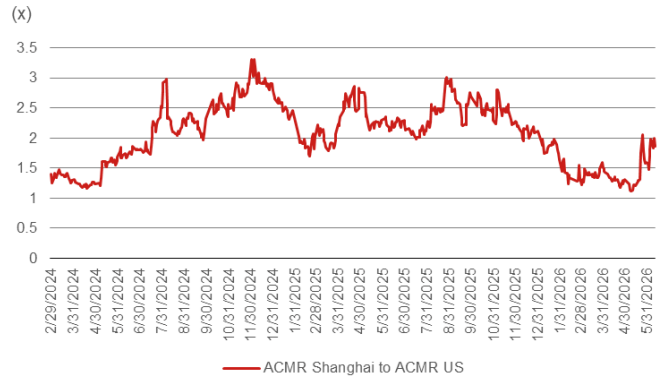
We initiate coverage of CXMT with a Buy rating with TP of CNY116 is based on 20x 2028F EPS of CNY5.8. Our 20x target P/E is based on: 1) the valuation in China being 1-3x higher than in the US market based on Bloomberg consensus numbers for ACMR Shanghai (688082 CH, Not rated) vs ACMR (ACMR US, rating suspended) (*Fig. 32*); and 2) Micron's historical two-year forward P/E range of around 5-15x with midpoint of 10x. Thus, if we assume CXMT is trading at 2x Micron's valuation (as we view Micron as one of CXMT's closest competitors), its P/E could be around 10-30x, with a midpoint of 20x (*Fig. 33*).

On the other hand, as CXMT's bit production growth is running at around 20% ahead of global DRAM bit growth for the coming year, on our estimates, we expect CXMT's market share would increase from the current ~10% to ~18% by end-2028F, which would result in a market share closer to Micron's 20%+. Thus, CXMT's market share could be approaching that of Micron's as time goes by. Micron currently is trading at USD960bn market cap (as of 20 July 2026).

Downside risks: 1) deteriorating server, PC, smartphone and automotive demand; 2) rising competition from domestic peers such as YMTC (unlisted), as YMTC is also developing DDR5 and could be ready for sampling by end-2026F, but initially it could be mainly for its internal SSD usage; 3) insufficient IC and components supply, such as CPU; and 4) rising geopolitical tensions between the US and China, which would put CXMT's business development, capacity expansion, and technology migration at risk.

Fig. 32: P/E multiple of ACMR Shanghai vs ACMR US

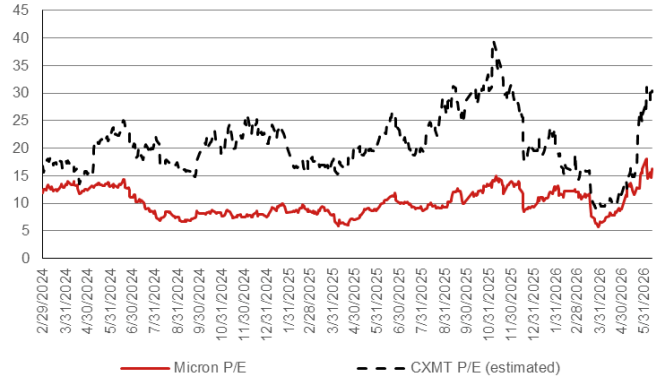
ACMR Shanghai's P/E is trading at 1-3x of ACMR US



Source: Bloomberg Finance L.P.

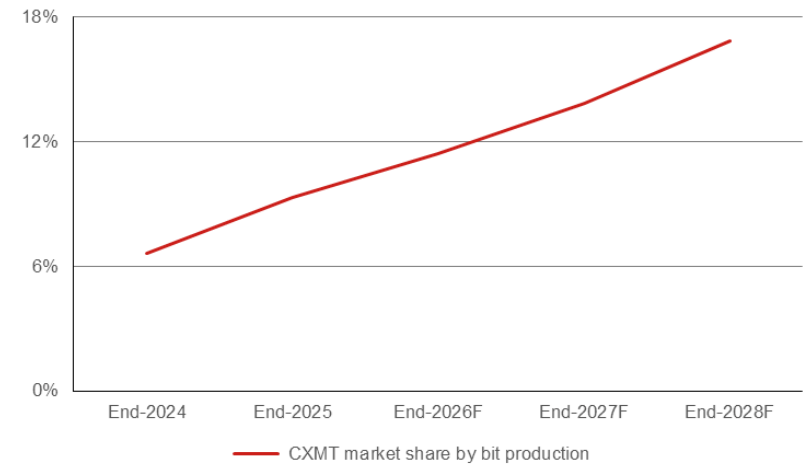
Fig. 33: Estimated P/E of CXMT based on Micron's

We assume CXMT's P/E is also likely trading at 1-3x of Micron's



Source: Bloomberg Finance L.P.

Fig. 34: CXMT: Market share by DRAM bit production



Source: Company data, Nomura estimates

Appendix: Manufacturing facilities, management team, and major shareholders

Company profile

CXMT Corporation (长鑫科技集团股份有限公司, was originally established in May 2016 as Hefei Ruili Integrated Circuit (合肥睿力集成电路). The company name was later changed to Innotron Memory and subsequently renamed ChangXin Memory Technologies in 2019, starting with 20kwpms capacity using a 19nm process for 8GB LPDDR4 and DDR4 DRAM production initially. Following a few years of expansion, CXMT has become China's largest and the world's fourth-largest DRAM manufacturer, and the only mainland Chinese company with mass-production capability for general-purpose DRAM, headquartered in Hefei, Anhui Province, China. CXMT operates as an IDM (Integrated Device Manufacturer), integrating chip design, wafer fabrication, packaging & testing, and product sales. The company's founder and Chairman, Zhu Yiming (朱一明), is also the controlling shareholder (at 2.6% pre-IPO stake) and founder of GigaDevice Semiconductor (603986 CH, Buy). CXMT has developed four generations of proprietary DRAM technology and its products include DDR4, DDR5, LPDDR4X, LPDDR5, and LPDDR5X, serving applications in mobile terminals, PCs, servers, AI, VR, and IoT. According to company, as of 2025, CXMT held approximately ~8% global DRAM market share, up from ~4% in 2024.

During the reporting period in 2022-25, CXMT's capacity utilization rate improved steadily from 85% to 95%. The company recorded cumulative losses of CNY8.32bn (2022), CNY16.3bn (2023), and CNY7.1bn (2024) before turning profitable in 2025 (net profit CNY18.7bn) as DRAM prices surged. In 1Q26, CXMT's revenue surged 719% y-y to CNY50.8bn, with net profit of CNY24.8bn, as DRAM prices rose sharply due to the continuous rise of global AI-driven demand. The company forecasts 1H26 revenue of CNY110-120bn and net profit of CNY50-57bn.

Facilities and offices

CXMT operates three DRAM wafer-fabrication plants across two cities (Hefei and Beijing), with a target to increase combined monthly capacity to 300kwpm by end of 2026. The company is also expanding an HBM (High Bandwidth Memory) production facility in Shanghai, targeting production by end-2026.

Fig. 35: CXMT: production facilities and offices

Facility Location	Wafer Size	Products	Use	Notes
Hefei, Anhui – Fab 1 (HQ)	12"	DDR4, DDR5, LPDDR4X, LPDDR5, LPDDR5X DRAM chips	Primary manufacturing, R&D, HQ	Primary production base; 17nm & 19nm process nodes; largest fab
Hefei, Anhui – Fab 2 (Changxin Xinqiao / 长鑫新桥)	12"	DDR4, DDR5, LPDDR series DRAM chips	Manufacturing	Newer fab; capacity ramping; CXMT holds 30.68% directly and controls 73.01% voting rights via acting-in-concert agreements with Hefei SASAC entities
Beijing – Fab 3 (Changxin Jidian / 长鑫集电)	12"	Advanced-node DRAM; next-gen process development (including HBM)	Advanced process R&D, Manufacturing	Focuses on more advanced process development; CXMT holds 31.72% directly + controls 75.32% voting rights via acting-in-concert agreements
Shanghai – HBM packaging including TSV (Xinputianyin Smart Technology / 芯浦天英)	—	HBM3 (High Bandwidth Memory) back-end packaging and testing	Advanced packaging	Under expansion; target production by end of 2026; entry into HBM market
Hefei, Anhui – R&D Center	—	DRAM circuit design, process R&D, product development	R&D	Core R&D hub
Other domestic offices	—	—	Sales, Service	Domestic sales and customer support network

Source: Company data, Nomura research

Management team and Board of Directors

CXMT's Board of Directors consists of 11 members: 7 non-independent directors and 4 independent directors. The company has no controlling shareholder and no actual controller.

Fig. 36: CXMT: management team and board of directors

Name	Occupation	Resume
Zhu Yiming (朱一明)	Chairman of the Board & CEO (Founder)	Founder of CXMT. Established the company in 2016 with state backing from Hefei municipal government. Also the controlling shareholder, actual controller and founder of GigaDevice Semiconductor Inc. (603986 CH, Buy), a leading NOR Flash and MCU company listed on the Shanghai Stock Exchange. Through Hefei Jixin No. 41 partnership (合肥集鑫肆拾壹号), Zhu holds approximately 1.536bn incentive shares in CXMT. As a long-term commitment, Zhu has voluntarily pledged to allocate 50% of his shares (~768mn shares) to future employee incentive programs (excluding himself), to be distributed over 5 years beginning 36 months after IPO. Zhu has also committed to a 10-year lock-up post-IPO, with gradual reduction of up to 20% per year in the second decade. Under his leadership, CXMT has developed four generations of DRAM technology and grown to become China's largest and the world's fourth-largest DRAM manufacturer.
Fang Wei (方纬)	Director	Board Director nominated by Changxin Jicheng (长鑫集成), the second-largest shareholder (11.71%). Represents the interests of the Hefei municipal state-owned capital entities on the board.
Other Non-Independent Directors (5)	Directors	Five additional non-independent directors serve on the board, nominated by various shareholder entities including Qinghui Jidian (清辉集电, largest shareholder at 21.67%), the National IC Fund Phase II (大基金二期, 8.73%), Anhui Province Investment (安徽省投, 7.91%), and other institutional shareholders. Per the prospectus, no single shareholder can determine the appointment of more than half of the board members.
Independent Directors (4)	Independent Directors	Four independent directors provide oversight on audit, governance and compliance. Their appointment ensures compliance with STAR Board listing requirements for independent board supervision.

Source: Company data, Nomura research

Major shareholders (pre-IPO)

CXMT has no controlling shareholder and no actual controller. The shareholding structure is dispersed, with a "four-pillar co-governance" structure comprising state-owned capital, the National IC Fund, industrial capital, and the founding team. The largest shareholder, Qinghui Jidian, is itself a partnership with no single controller – its executive partner Qinghui Changxin (清辉长鑫, 0.01% of Qinghui Jidian) is controlled by Chairman Zhu Yiming, while Xinrui Investment (芯睿投资, 51.09%) is controlled by Hefei Economic Development Zone SASAC, and Changxin Jicheng (长鑫集成, 48.90%) is controlled by Hefei SASAC. Combined Hefei state-owned entities hold approximately 35% of CXMT.

Fig. 37: CXMT: Major shareholders (pre-IPO)

Holder Name	Position (%)	Nature / Notes
Qinghui Jidian (清辉集电) – Largest shareholder	21.67%	Limited partnership; no single controller. Controlled jointly by Zhu Yiming (via Qinghui Changxin), Hefei EDZA SASAC (via Xinrui Investment), and Hefei SASAC (via Changxin Jicheng)
Changxin Jicheng (长鑫集成) – Hefei SASAC entity	11.71%	Controlled by Hefei Municipal SASAC; also holds 48.90% of Qinghui Jidian
National IC Industry Investment Fund Phase II (大基金二期)	8.73%	China's national semiconductor fund (Big Fund II); entered in A-round financing
Hefei Jixin (合肥集鑫) – Employee incentive platform	8.37%	Partnership vehicle through which founder Zhu Yiming holds ~1.536 billion incentive shares
Anhui Province Investment Group (安徽省投)	7.91%	Controlled by Anhui Provincial SASAC
GigaDevice Semiconductor (兆易创新, 603986 CH, Buy)	~1.88%	Strategic partner; DRAM foundry customer; invested RMB 1.5 billion in 2024 at ~RMB 140 billion pre-money valuation
Other notable investors	Various	Include Alibaba, Tencent/Hubei Xiaomi, CCB International (建银国际), ABC Financial (农银金融), China Life Investment (国寿投资), PICC Capital (人保资本), Legend Capital (君联资本), Guotiao Fund (国调基金), among others across nine funding rounds
Hefei state-owned entities (combined)	~35%	Aggregate of Qinghui Jidian, Changxin Jicheng, Hefei Chantou, and related SASAC entities

Source: Company data, Nomura research

Appendix A-1

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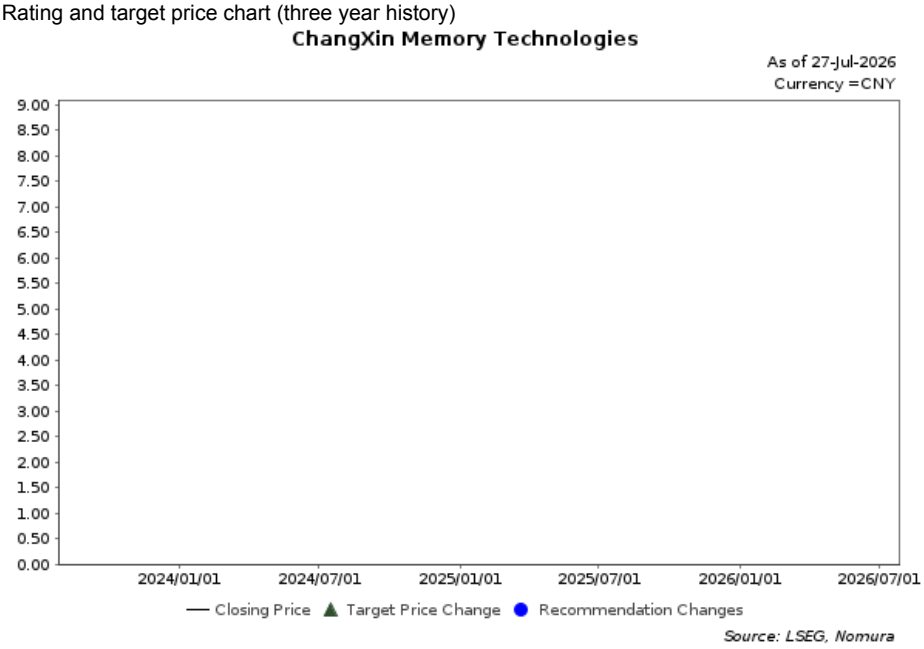
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Materially mentioned issuers

Issuer	Ticker	Price	Price date	Stock rating	Sector rating	Disclosures
ChangXin Memory Technologies	688825 CH	CNY 8.66	27-Jul-2026	Buy	N/A	

ChangXin Memory Technologies (688825 CH) **CNY 8.66 (27-Jul-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)



Date	Rating	Target price	Closing price

For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology Our TP CNY116 is based on 20x 2028F EPS of CNY5.8. We assign a 20x target P/E multiple as we expect CXMT to trade twice the valuation of its major US competitor, Micron, which has traded at ~10x over the past five years, due to CXMT's market share gains and the higher valuation multiples in the China market. The benchmark index is CSI300
Risks that may impede the achievement of the target price Downside risks include: (1) worsening of end demand; (2) intensifying competition from domestic peers such as YMTC; (3) insufficient supply of IC and components such as CPUs; and (4) escalation of geopolitical tensions between the US and China.

Important Disclosures

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STOCKS

A rating of **'Buy'**, indicates that the analyst expects the stock to outperform the Benchmark over the next 12 months. A rating of **'Neutral'**, indicates that the analyst expects the stock to perform in line with the Benchmark over the next 12 months. A rating of **'Reduce'**, indicates that the analyst expects the stock to underperform the Benchmark over the next 12 months. A rating of **'Suspended'**, indicates that the rating, target price and estimates have been suspended temporarily to comply with applicable regulations and/or firm policies. Securities and/or companies that are labelled as **'Not rated'** or shown as **'No rating'** are not in regular research coverage. Investors should not expect continuing or additional information from Nomura relating to such securities and/or companies. Benchmarks are as follows: **United States/Europe/Asia ex-Japan:** please see valuation methodologies for explanations of relevant benchmarks for stocks, which can be accessed at: http://go.nomuranow.com/research/m/Disclosures; **Global Emerging Markets (ex-Asia):** MSCI Emerging Markets ex-Asia, unless otherwise stated in the valuation methodology; **Japan:** Russell/Nomura Large Cap.

SECTORS

A **'Bullish'** stance, indicates that the analyst expects the sector to outperform the Benchmark during the next 12 months. A **'Neutral'** stance, indicates that the analyst expects the sector to perform in line with the Benchmark during the next 12 months. A **'Bearish'** stance, indicates that the analyst expects the sector to underperform the Benchmark during the next 12 months. Sectors that are labelled as **'Not rated'** or shown as **'N/A'** are not assigned ratings. Benchmarks are as follows: **United States:** S&P 500; **Europe:** Dow Jones STOXX 600; **Global Emerging Markets (ex-Asia):** MSCI Emerging Markets ex-Asia. **Japan/Asia ex-Japan:** Sector ratings are not assigned.

Target Price

A Target Price, if discussed, indicates the analyst's forecast for the share price with a 12-month time horizon, reflecting in part the analyst's estimates for the company's earnings. The achievement of any target price may be impeded by general market and macroeconomic trends, and by other risks related to the company or the market, and may not occur if the company's earnings differ from estimates.

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