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Memory Interface Chip Primer: Riding on the agentic AI boom


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We initiated coverage on Montage in April (initiation report and deck) where we discuss the opportunity for memory interface chip vendors driven by agentic AI. In this primer, we provide a comprehensive overview of the industry's growth drivers, competitive dynamics, and investment implications to help investors navigate the sector. Updated models can be downloaded here: Memory Interface Chip Industry Model and Montage Model. **Reiterate Outperform on Montage**, PT revised up from HKD 320 to 520 in H-share and CNY 220 to 400 in A-share. **Reiterate Outperform on Renesas.**

Memory interface chips are a direct and amplified beneficiary of the server CPU Renaissance driven by Agentic AI. As the industry shifts from GPU-centric training toward inference-heavy agentic AI deployments—where the CPU reclaims its role as orchestrator of multistep, sequential tasks—server CPU volumes are poised to grow structurally faster than expected (our CPU report), and the role of memory interface chip becomes increasingly important when the DRAM capacity and bandwidth per CPU grows. We project the global memory interface chips TAM to reach USD 20Bn by 2030 (3x of our previous projection) at 65% CAGR (vs 32%), driven by three reinforcing tailwinds: rising server CPU volume, increasing DRAM package count per CPU, and higher interface chip content per package through the MRDIMM upgrade.

MRDIMM penetration is an important driver, as interface chip value per MRDIMM module is roughly 10× that of RDIMM. Each MRDIMM adopts a "1 MRCD+10 MDB" architecture, versus just one RCD in standard DDR5 RDIMM. We project MRDIMM penetration to reach 25% (vs 20% previously) of global server DDR DIMM shipments by 2030, driven by the bandwidth improvement MRDIMM delivers. The adoption hurdle is manageable: MRDIMM premium is only about 10% of the current 128GB RDIMM price, and this gap narrows further as rising DRAM die prices reduce the premium.

The competitive landscape for core memory interface chips is a textbook oligopoly that drives high margin. Montage, Renesas, and Rambus (RMBS, not covered) collectively control 90%+ of global share, protected by rigorous JEDEC qualification cycles and deep co-development ties with DRAM IDMs and CPU platforms. The chip is crucial for the package performance but takes only LSD% of the package price, customers have very low incentive to shift to new vendors and are willing to offer high margin to secure the quality. The three vendors compete neck-and-neck on the RDIMM roadmap, while Renesas and Montage hold early-mover advantages in MRDIMM. The complementary supporting chips segment is more fragmented, where Renesas leads thanks to its analog heritage.

We favor all three leading suppliers, as market has not fully priced in upside from CPU acceleration and MRDIMM adoption. We raise Montage TP to CNY400/ HKD520 for A-/H-Share, supported by CPU-driven demand across both its memory interface and PCIe businesses, as well as share gains from CXMT expansion. **Renesas**'s memory interface is at a scale similar to Montage's despite contributing only 6% of it revenue, yet its market cap is only 25% above Montage's; it appears significantly undervalued, and management's guidance for 20-30% growth CAGR for this business is too low. **Rambus** benefits across both interface chip products and memory controller IP royalties; its smaller revenue base and market cap give it the largest potential upside elasticity.

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BERNSTEIN TICKER TABLE

			8 Jul 2026		TTM	Reported EPS				Reported P/E (x)		
Ticker	Rating	Cur	Closing Price	Price Target	Rel. Perf.	Cur	2025A	2026E	2027E	2025A	2026E	2027E
688008.CH (Montage)	O	CNY	247.15	**400.00**	169.8%	CNY	1.97	**3.21**	**5.68**	125.5	77.1	43.5
OLD				220.00				3.00	4.77			
6809.HK (Montage)	O	HKD	321.40	**520.00**	NA	CNY	1.97	**3.21**	**5.68**	141.4	86.9	49.1
OLD				320.00				3.00	4.77			
6723.JP (Renesas)	O	JPY	4,662.00	6,300.00	93.0%	JPY	181.61	244.76	298.54	25.7	19.0	15.6
ASIAX			1,945.70									
JPL			2,651.83									

PRICE TARGET CHANGE / ESTIMATE CHANGE IN BOLD

O - Outperform, M - Market-Perform, U - Underperform, NR - Not Rated, CS - Coverage Suspended

6723.JP estimate is Adjusted EPS; 6723.JP valuation is Adjusted P/E (x);

Source: Bloomberg, Bernstein estimates and analysis.

INVESTMENT IMPLICATIONS

Since April the shares of Montage, Rambus, and Renesas have rallied for several months, reflecting strong investor interest in the memory interface chip sector as the CPU vendors comment on strong server CPU demand. Over the past month, however, their share prices have corrected 10–30% from peak levels as investors increasingly question whether valuations have become overstretched. We expect sentiment to remain weak in the near term, reflecting continued softness in memory-related sentiment, profit-taking following the strong share price rally, and concerns around weak near-term earnings due to substrate shortage for Montage and Rambus. From a tactical perspective, investors may prefer to remain on the sidelines for the near term. However, we expect that on a 12-month horizon, as the MRDIMM penetration continue to increase, when investor start to look into the potential upsides in 2028 then the stocks could work again, therefore long-onlys should look to buy the dip when the market corrects.

Montage Technology: We rate Montage Technology as **Outperform** and raise our **A-share TP to CNY 400**, based on **50x 2BF P/E** (27Q3–28Q2 earnings). We believe a 2BF framework better reflects the upcoming earnings inflection driven by the 2027–2028 product cycle, including the ramp-up of MRDIMM interface chips, and the P/E is lower than the 5-year CAGR so should have more upside as well. We raise our 2027/2028 EPS estimates by 19%/73%, respectively, on a stronger outlook for the CPU cycle and better MRDIMM penetration. We also increase our target multiple from 44x to 50x, supported by the rapid growth of the ESP business (76.5% CAGR2025–28). For the **H shares**, we set a target price of **HKD 520**, implying a **15% premium** to our A-share TP (we use the CNY to HKD exchange rate at 1:1.13). The H share premium reflects that global investors favor Montage as a scarce China AI-exposed name without direct geopolitical risks, unlike many other Chinese semiconductor companies that face entity list restrictions or export control headwinds. At our target price, the implied P/E multiple on 2BF EPS for H shares is 58x. H share has limited free float due to lock up, so we still expect H share premium to maintain at high level for the near term. After lock-up period, the H share premium could start to narrow again.

Renesas: We are constructive on AI data center semiconductors *(refer to Artificial Intelligence - Energizing the Future of AI Data Centers and Global Semis: The CPU Renaissance? Beneficiaries of a $223bn TAM)*. Within Renesas' AI infrastructure portfolio, we see both power semiconductors and memory interface ICs as attractive growth drivers. We forecast AI infrastructure revenue to account for 27% of Renesas' total revenue by 2028, vs.11% in 2025 *(refer to Infineon/Renesas: CPU renaissance emerges as a second engine for power semi demand, set to outstrip supply)*. We rate Renesas **Outperform**, with PT = **¥6,300.00**.

EXHIBIT 1: **Montage Bern. forecast vs. Consensus vs. Bern Old**

Revenue (RMB mn)	2023	2024	2025	2026E	2027E	2028E	2029E	2030E
Bernstein	**2,286**	**3,639**	**5,456**	**7,733**	**13,552**	**25,211**	**41,966**	**58,298**
Growth YoY	(38%)	59%	50%	42%	75%	86%	66%	39%
Consensus	**2,286**	**3,639**	**5,456**	**7,448**	**10,752**	**13,656**		
Growth YoY			50%	36%	44%	27%		
Bernstein vs. consensus				3.8%	26.0%	84.6%		
Bernstein old				**7,793**	**11,688**	**14,941**	**20,420**	**25,508**
New vs. Old				(0.8%)	16.0%	68.7%	105.5%	128.6%
Gross profit								
Bernstein	**1,347**	**2,115**	**3,395**	**5,233**	**8,988**	**16,378**	**26,537**	**35,832**
Growth YoY		57%	61%	54%	72%	82%	62%	35%
GP Margin	58.9%	58.1%	62.2%	67.7%	66.3%	65.0%	63.2%	61.5%
Consensus	**1,347**	**2,115**	**3,395**	**5,264**	**7,817**	**9,969**		
Growth YoY		57%	61%	55%	48%	28%		
GP Margin			62.2%	70.7%	72.7%	73.0%		
Bernstein vs. consensus - GP				(0.6%)	15.0%	64.3%		
Bernstein vs. consensus - GPM				(301bps)	(638bps)	(804bps)		
Bernstein old				**5,168**	**7,828**	**10,191**	**14,183**	**18,004**
New vs. Old				1.3%	14.8%	60.7%	87.1%	99.0%
Operating profit								
Bernstein	**199**	**1,046**	**1,971**	**3,531**	**6,943**	**13,962**	**23,681**	**32,491**
Growth YoY		426%	88%	79%	97%	101%	70%	37%
OP Margin	8.7%	28.8%	36.1%	45.7%	51.2%	55.4%	56.4%	55.7%
Consensus	**199**	**1,046**	**1,971**	**3,534**	**5,185**	**6,960**		
Growth YoY		426%	88%	79%	47%	34%		
OP Margin			36.1%	47.5%	48.2%	51.0%		
Bernstein vs. consensus - OP				(0.1%)	33.9%	100.6%		
Bernstein vs. consensus - OPM				(179bps)	301bps	441bps		
Bernstein old				**3,517**	**5,868**	**7,931**	**11,576**	**15,010**
New vs. Old				0.4%	18.3%	76.0%	104.6%	116.5%
Net income attributable to shareholders								
Bernstein	**451**	**1,412**	**2,236**	**3,721**	**6,594**	**12,706**	**21,071**	**28,545**
Growth YoY	(65%)	213%	58%	66%	77%	93%	66%	35%
NP Margin	19.7%	38.8%	41.0%	48.1%	48.7%	50.4%	50.2%	49.0%
Consensus	**451**	**1,412**	**2,236**	**3,562**	**5,246**	**7,383**		
Growth YoY			58%	59%	47%	41%		
NP Margin	19.7%	38.8%	41.0%	47.8%	48.8%	54.1%		
Bernstein vs. consensus - NP				4.5%	25.7%	72.1%		
Bernstein vs. consensus - NPM				30bps	(13bps)	(366bps)		
Bernstein old				**3,628**	**5,769**	**7,645**	**10,877**	**13,908**
New vs. Old				3%	14%	66%	94%	105.2%
Basic EPS								
Bernstein		**1.25**	**1.97**	**3.21**	**5.68**	**10.82**	**17.93**	**24.04**
Growth YoY			58%	63%	77%	91%	66%	34%
Consensus		**1.25**	**1.97**	**3.02**	**4.36**	**6.09**		
Growth YoY			58%	53%	44%	40%		
Bernstein vs. consensus				6.2%	30.3%	77.8%		
Bernstein old				**3**	**5**	**6**	**9**	**11**
New vs. Old				7%	19%	73%	102%	113.7%

Source: Bloomberg, Bernstein analysis and estimates

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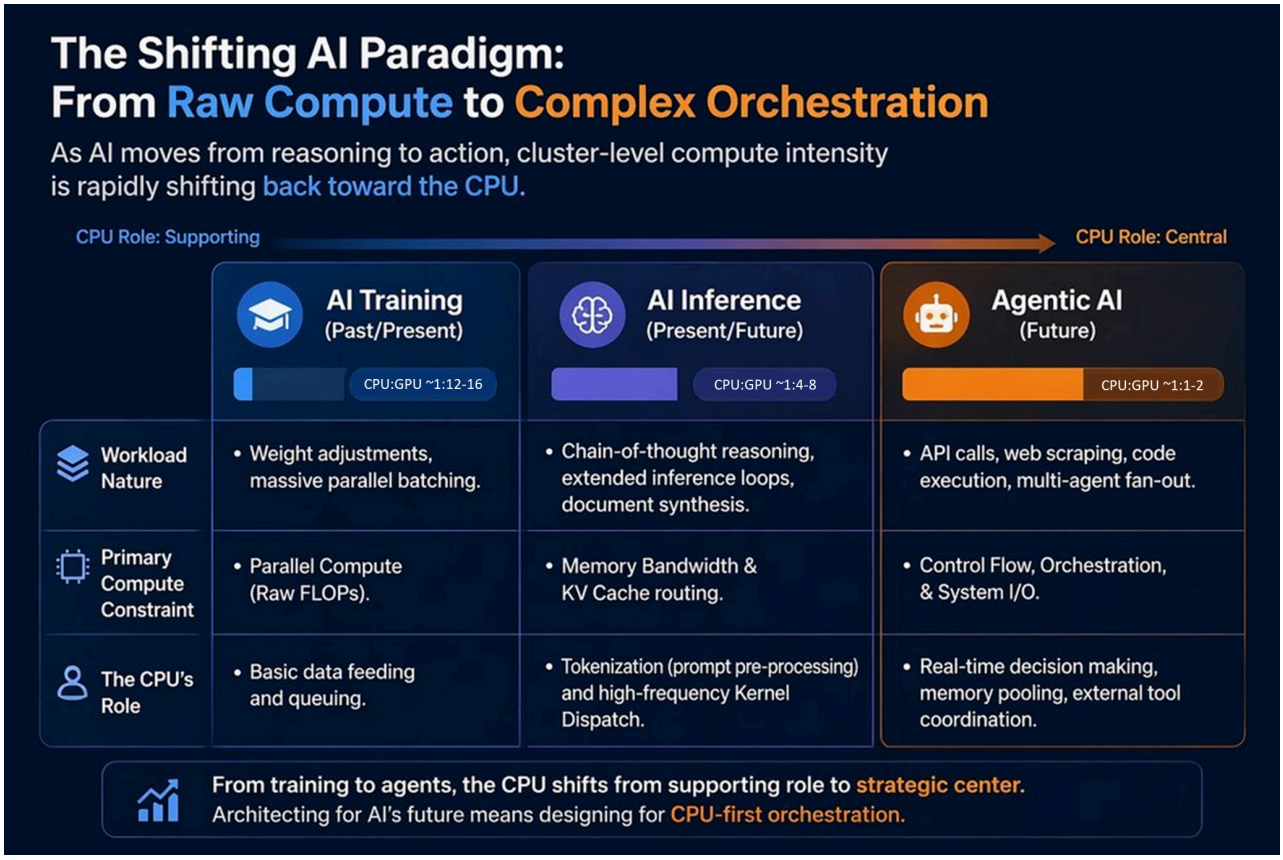
DETAILS

MEMORY INTERFACE CHIP: CORE BENEFICIARY IN THE AGENTIC AI ERA

Agentic AI is structurally reshaping the demand for server CPUs, DDR memory, and the interface chips that connect them. Three compounding tailwinds — rising CPU volumes, more DRAM per CPU, and a rise in chipset value through the MRDIMM upgrade — drive the memory interface chip TAM to grow at ~65% CAGR2025-2030.

The AI industry is entering a new phase. As workloads shift from training to inference and agentic applications, compute intensity is migrating back toward the server CPU. In training, GPUs handle massive parallel computing workloads while CPUs sit largely idle. As AI moves from reasoning to action, the workload becomes multistep, sequential, and time-sensitive, precisely the domain where CPUs excel. The CPU becomes the essential orchestrator: it schedules thousands of small computational tasks to the GPU every second, manages the model's working memory (KV cache), executes real-time safety checks, and coordinates API calls to external tools. In these workloads, CPU-side processing can account for 50–90% of total task completion time. The CPU-to-GPU ratio shifts dramatically, reaching approximately 1:1-2 in agentic architectures. AMD recently doubled its projection for the global (x86) server CPU TAM to USD 120 billion by 2030 compared to the projection in last quarter's earnings, reflecting rapidly rising expectations for CPU demand. Every additional server CPU shipped requires multiple DDR memory modules, each populated with memory interface chipsets.

EXHIBIT 2: **As AI transitions from a training-heavy era (dominated by GPUs) to an inference-heavy era, the role of CPUs expands. Training requires parallel processing, but inference and specifically agentic workflows requires the sequential and latency-sensitive capabilities of CPUs**



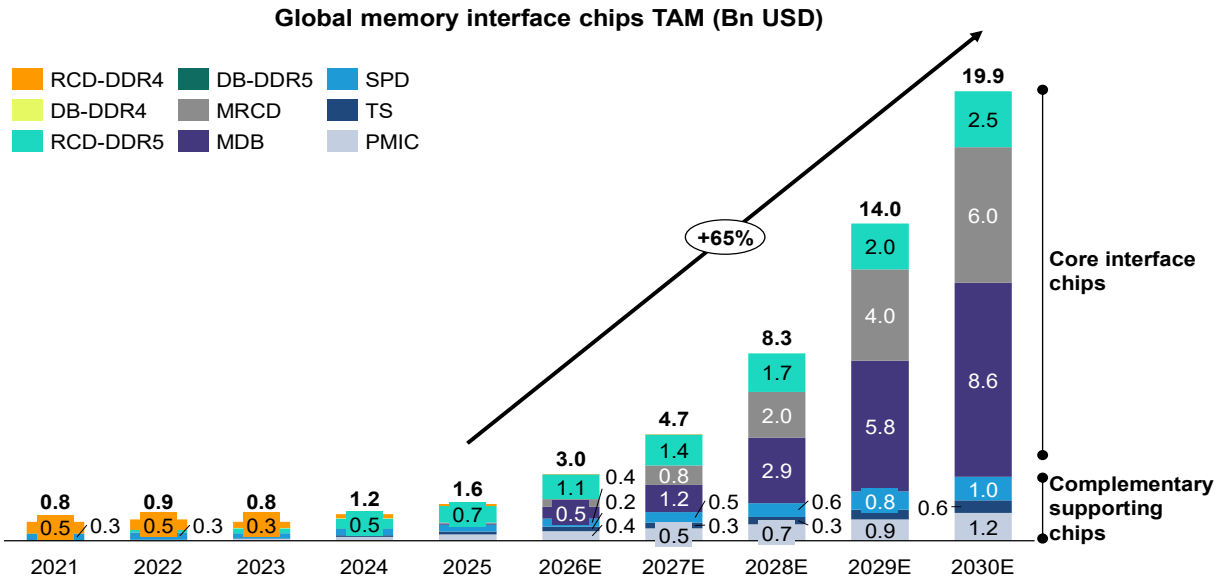
The CPU-to-GPU ratios are illustrative here, subject to change in various server architectures
Source: public reports, Bernstein analysis and estimates

Agentic AI workloads demand substantially more memory bandwidth and capacity than prior generations, for KV cache storage, context windows, and working memory that grows with task complexity. The industry is responding by increasing the number of DDR channels per CPU (migrating from 8 to 12 and eventually 16 channels) and by fully populating DIMM slots in AI servers to maximize accelerator utilization. More DRAM modules per server means proportionally more memory interface chips per server — a structural multiplier that compounds on top of the CPU volume growth.

Bandwidth starvation of agentic AI are accelerating the transition from DDR5 RDIMM to DDR5 MRDIMM, which increases the memory interface chip value per module by roughly 10×. As data rates push beyond 8800 MT/s — driven by the same AI workloads demanding higher memory bandwidth — conventional RDIMM architectures hit fundamental signal integrity limits. MRDIMM resolves this through active signal retiming, requiring one MRCD plus ten MDB chips per module versus a single RCD for RDIMM. This is not an incremental improvement; it is a step-change in silicon content per server that transforms the economics of the entire memory interface chip market.

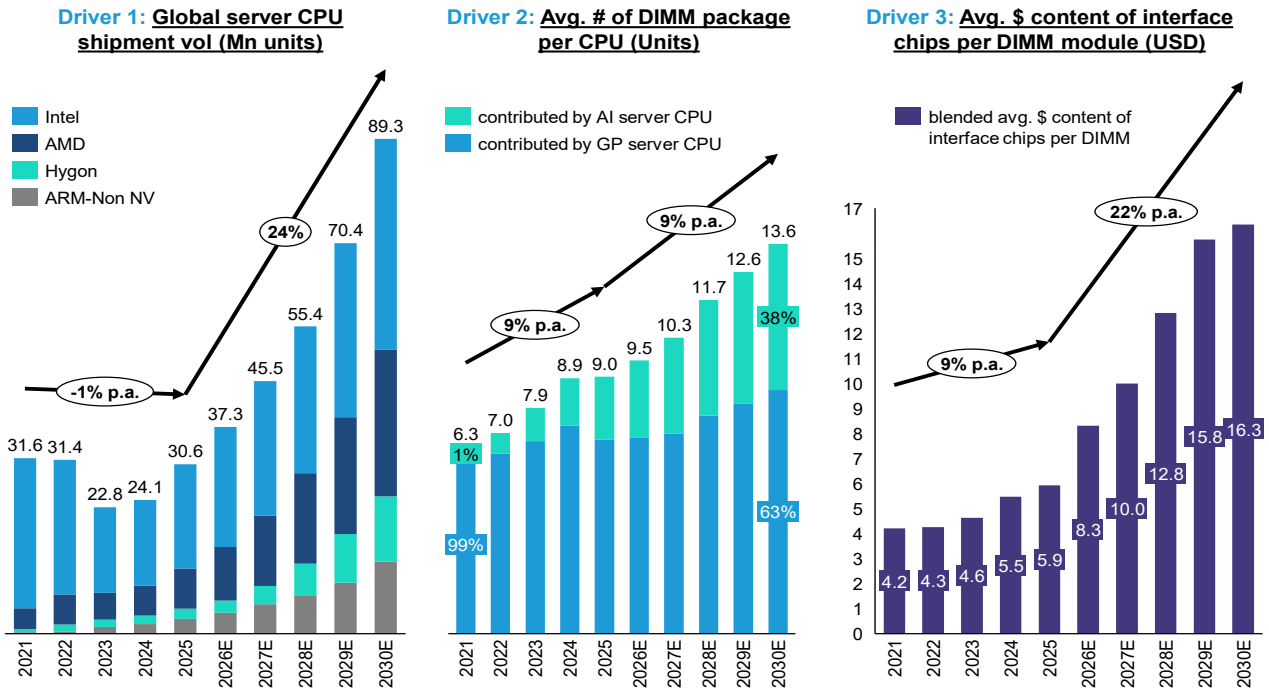
These three forces are multiplicative, not additive. The TAM is the product of CPU volumes, DRAM modules per CPU, and chipset value per module, nearly all of which are rising simultaneously. This structural alignment explains why we project the global DDR module chipset TAM to reach USD 20Bn by 2030 (~65% CAGR), dramatically outpacing the ~24% growth in server CPU shipments, making the sector almost 3x more elastic on top of the CPU vol growth. Note that the TAM is both sensitive to the CPU volume and MRDIMM penetration, as we highlighted in Exhibit 5, so if the CPU market didn't grow as fast as expected and MRDIMM penetration was lower than projected, there is downside risk to our projections.

EXHIBIT 3: **We raise our global memory interface TAM projection to USD 20Bn in 2030, with MRDIMM's MRCD and MDB contributing 73%, driven by significantly higher chipset value per module**



Our TAM forecast does not include memory interface chips used in NVIDIA proprietary CPUs, such as voltage regulators and PMICs. We expect the impact to be only LSD, as NVIDIA CPUs account for a small portion of server CPU shipments and the related components are of relatively low value.
Source: Mercury, TrendForce, Gartner, Bernstein analysis and estimates

EXHIBIT 4: **The expansion of the TAM is driven by three core factors, each of which is expected to accelerate in the second half of this decade relative to the past 5 years**



Source: Gartner, Mercury, Bernstein analysis and estimates

EXHIBIT 5: **2030 TAM Sensitivity Analysis: Even in a bear-case scenario, the global memory interface chip TAM reaches our prior-version projection, reinforcing a well-protected downside for Montage at current share price**

2030 TAM sensitivity analysis (Bn USD)		***Server CPU shipment in 2030 (excl. NV, Mn units)***						
		60	70	80	89	100	110	120
MRDIMM penetration in 2030	10%	8	9	10	12	13	14	16
	15%	10	11	13	14	16	18	19
	20%	12	13	15	17	19	21	23
	25%	13	16	18	20	22	24	27
	30%	15	18	20	23	25	28	30
	35%	17	20	23	25	28	31	34
	40%	19	22	25	28	32	35	38

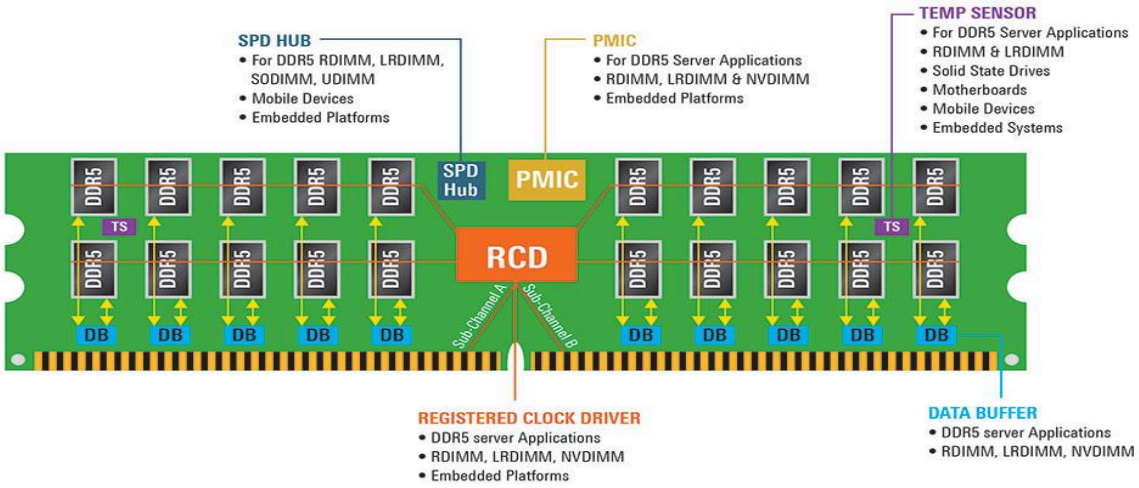
Source: Bernstein analysis and estimates

PRODUCT PRIMER: MEMORY MODULE AND MEMORY INTERFACE CHIPS

DDR module chipsets are a family of specialized ICs mounted on server DIMM modules. They divide into two tiers — high-value memory interface chips (RCD, DB, MRCD, MDB) and complementary supporting chips (SPD, TS, PMIC) — with silicon content per module increasing dramatically across DDR generations and DIMM formats. Memory interface chips are the core high-value silicon, and Complementary supporting chips have grown in relevance since the DDR5 generation.

EXHIBIT 6: **DDR module chipset consists of two tiers of IC, Memory interface chips and Complementary supporting chips**

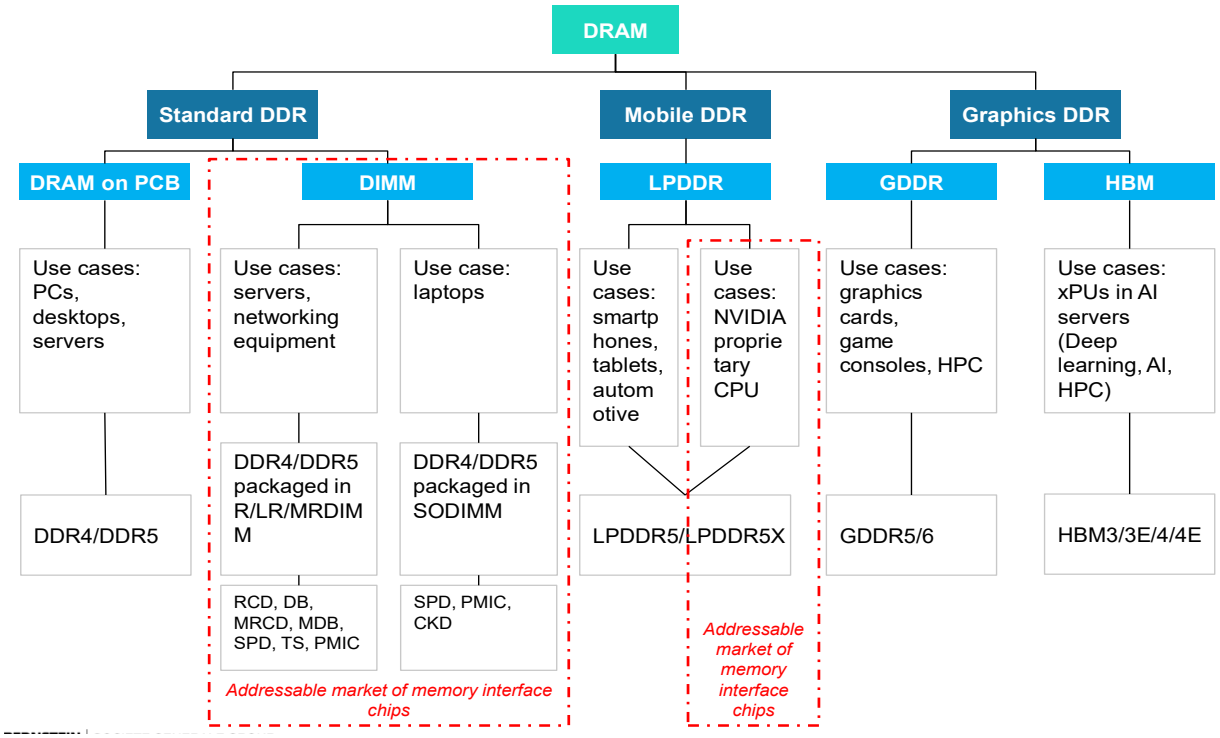
Memory interface chips	**Core interface chips**	• RCD: registered clock driver, compatible with RDIMM • DB: data buffer, compatible with RDIMM • MRCD: multiplexed rank registering clock driver, compatible with MRDIMM • MDB: multiplexed data buffer, compatible with MRDIMM
	Complementary supporting chips	• SPD: serial presence detect • PMIC: power management IC • TS: temperature sensor • CKD: clock driver, compatible with SODIMM/ UDIMM in PC



Source: Renesas, Bernstein analysis

Not all DRAM packages require memory interface chips. In PCs and low-end servers, where memory capacity and bandwidth requirements are modest, the CPU's integrated memory controller can communicate directly with DRAM chips without intermediary buffering. However, in high-end servers, particularly AI servers that demand maximum memory bandwidth and capacity, the CPU cannot talk to too many DRAMs simultaneously without signal degradation. This is where DDR module chipsets become essential.

EXHIBIT 7: **Among all DRAM variants, DDR packaged in DIMMs requires RCD/MRCD and DB/MDB to interface with server CPUs, while LPDDR used by NVIDIA Vera CPUs also needs some simplified memory interface chips**



Source: Semiconductor Engineering, Bernstein analysis

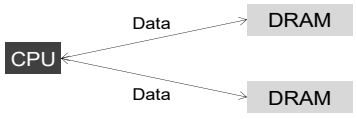
CORE INTERFACE CHIPS

Core interface chips are the most technically sophisticated and commercially valuable components in the DDR module chipset. They sit physically between the CPU memory controller and the DRAM dies on the module, buffering and conditioning signals to enable higher memory capacity and bandwidth than would otherwise be possible. A useful analogy: if the CPU is the "CEO" of a company, the RCD/MRCD is the "manager" that directs instructions, and the DB/MDB is the "delivery person" that physically moves data to and from the DRAM workforce.

EXHIBIT 8: **Memory interface chip: core networking chip to connect CPU and DRAM in servers to support more memory capacity/bandwidth**

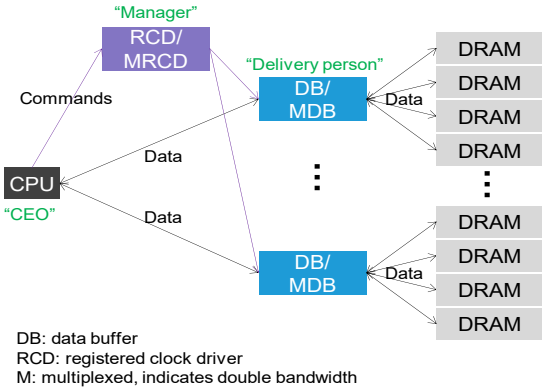
DRAM for PC and low-end servers: CPU connect to DRAM directly

- Limited requirement on the DRAM capacity/bandwidth
- CPU can talk to DRAM directly for data read/write



DRAM for high-end servers: CPU connect to DRAM through interface chips

- More DRAM capacity/bandwidth needed, especially for AI servers, but CPU as the "CEO" cannot talk to too many DRAMs at the same time
- **DB/MDB** as the additional "delivery person" to help CPU distribute and deliver the data to more DRAM
- **RCD/MRCD** as the additional "manager" to control the DB/MDB when and which to send data to CPU



Source: company reports, Bernstein analysis

RCD (Registered Clock Driver): The RCD is the bridge between the memory controller and the DRAM chips on the module. It provides command, address, and clock signals to achieve synchronous data transfer. RCDs are employed on RDIMM and LRDIMM server modules to enable higher capacity and better reliability than PC modules (UDIMM and SODIMM). One RCD is mounted per RDIMM module. The main functional blocks on a typical RCD chip include a logic microcontroller (usually ARM-based) for managing I/O ports, an I2C/I3C interface for inter-chip communication, and a clocking block for handling reference signals.

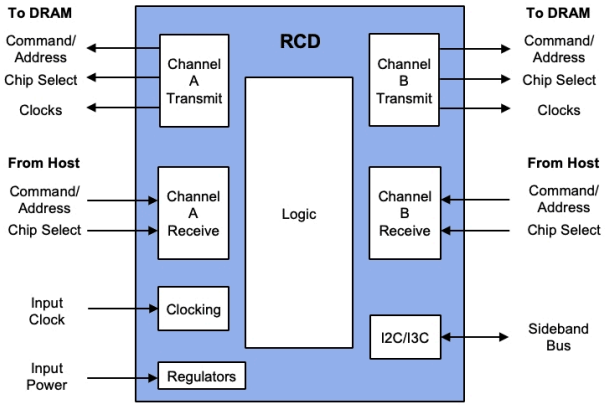
MRCD (Multiplexed Rank RCD): The MRCD is the next-generation registering clock driver designed specifically for DDR5 MRDIMM modules. Unlike conventional RCDs that passively buffer signals, the MRCD actively reshapes and re-clocks signals, maintaining signal integrity at the higher data rates that MRDIMM targets (8800–12800 MT/s). One MRCD is mounted per MRDIMM module.

RCDs/ MRCDs are the most complex and advanced ICs among the DIMM chipset. They were first introduced with DDR3 and have gained relevance with each subsequent generation. The leading vendors typically manufacture their RCDs using TSMC's CMOS processes, with DDR4 RCDs on 40nm platforms and DDR5 first-generation RCDs starting at 28nm. Future generations will migrate toward even more aggressive nodes (down to 10nm class) to support higher data rates.

DB (Data Buffer): Data buffers store copies of data blocks being transferred between the CPU and the DRAM dies. Positioned spatially closer to the DRAM chips than RCDs, they reduce I/O trace lengths, leading to less pronounced signal reflection and lower data load on the module's data bus. Consequently, modules with data buffers (LRDIMMs) can support higher memory capacities than RDIMMs. Data buffers were first implemented on DDR4 LRDIMMs, with 9 per module. Since JEDEC defines a specific number of DBs per module, they are sold in bundles to memory module vendors.

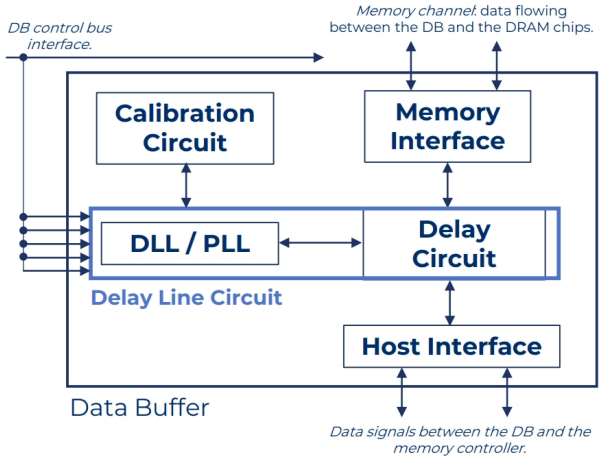
MDB (Multiplexed Rank Data Buffer): The MDB is the next-generation data buffer for DDR5 MRDIMM. Like the MRCD, it actively manages data signals through multiplexing, enabling concurrent access to two memory arrays on the module, effectively doubling per-module bandwidth versus conventional RDIMM. 10 MDBs are mounted per MRDIMM module, representing a dramatic increase in silicon content compared to DDR5 RDIMM, where no data buffers are required at 6400 MT/s.

EXHIBIT 9: **Logic diagram for RCD, including a MCU**



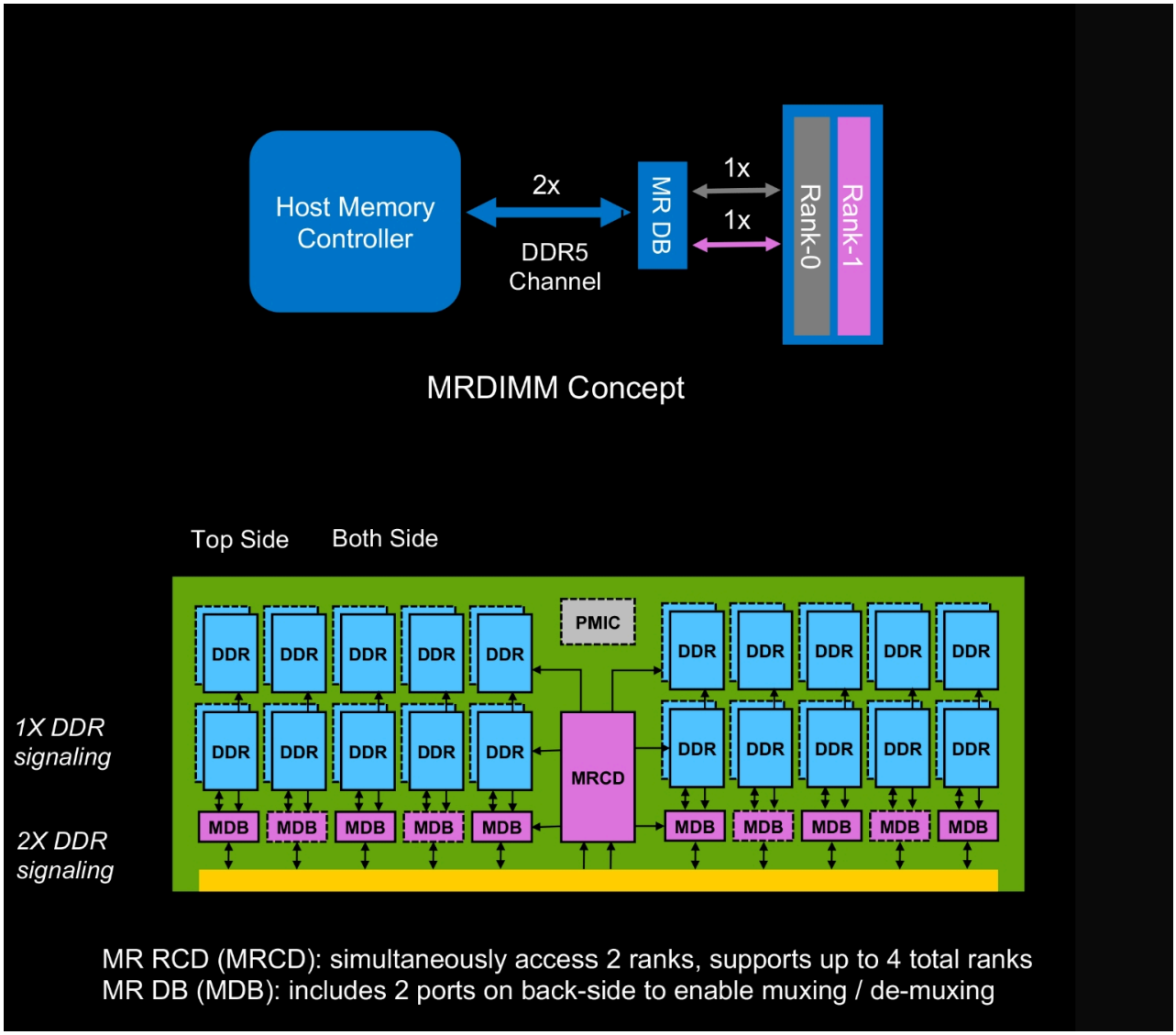
Source: Rambus

EXHIBIT 10: **Logic diagram for DB chips**



Source: JEDEC, Patent US10082823B1 by Renesas

EXHIBIT 11: **The mechanism of MRCD and MDB in MRDIMM: MRCD allows simultaneous access to both ranks, and MDB enables muxing and demuxing. Hence, two DDR ranks run in a multiplexed mode to double the speed**



Source: Micron, Bernstein analysis

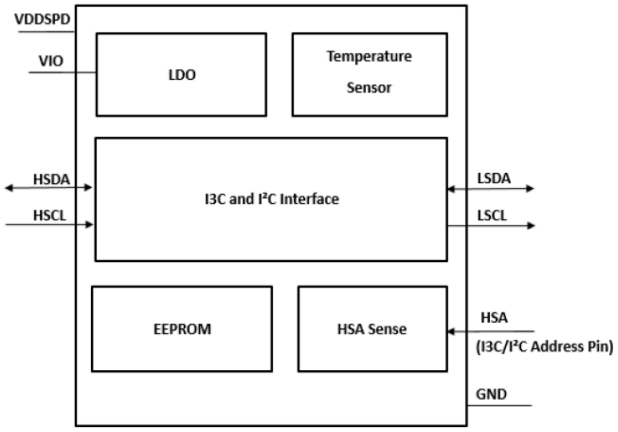
COMPLEMENTARY CHIPS

The DDR5 specification introduced several new on-module components that were absent in DDR4, expanding the total chipset content per module and creating additional revenue opportunities for chipset suppliers.

SPD Hub (Serial Presence Detect): The SPD Hub stores module configuration information — including size, speed, voltage, and timing parameters — that is read by the system BIOS during boot. It contains an embedded temperature sensor and manages the standalone temperature sensors mounted on the DIMM. A 1KB EEPROM device is also included to store DIMM topology configuration and DRAM information. One SPD Hub is present on every server DDR module across all formats and generations.

TS (Temperature Sensor): DDR5 temperature sensors must achieve approximately 0.25°C accuracy to trigger effective thermal management actions, including lowering IC speed or increasing cooling fan activity. Two standalone temperature sensors are mounted on each DDR5 server module (RDIMM and MRDIMM), compared to zero standardized sensors on DDR4 RDIMM modules. The sensors are managed by the SPD Hub through the I3C serial bus.

EXHIBIT 12: **DDR5 module introduces a SPD Hub, which stores configuration information in the EEPROM**



Source: Renesas

EXHIBIT 13: **DDR5 temperature sensors must achieve ~0.25 °C accuracy to trigger effective thermal management actions, including lowering IC speed or increasing cooling**

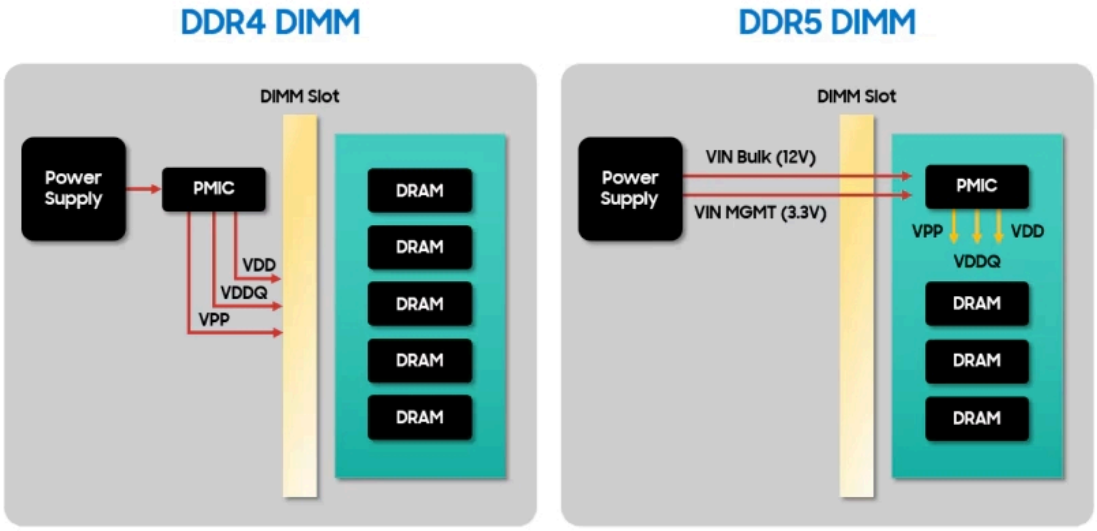
Temperature Sensor Performance

Parameter	Min	Typ	Max	Unit	Test Conditions
Temperature Sensor Accuracy (Active Range)	--	0.5	1.0	°C	75°C≤T_A≤ 95°C
Temperature Sensor Accuracy (Monitor Range)	--	1.0	2.0	°C	40°C≤T_A≤ 125°C
Temperature Sensor Accuracy (Industrial Temperature Range)	--	2.0	3.0	°C	-40°C≤T_A≤ 125°C
Resolution		0.25		°C	
Conversion Time			125	ms	Assumes 0.25°C accuracy
Hysteresis between temperature events	1	-	-	°C	

Source: Samsung, Bernstein analysis

PMIC (Power Management IC): The transition to DDR5 moved power regulation from the motherboard to the DIMM module itself. DDR5 PMICs include step-down switching regulators and low-dropout regulators to manage voltage conversion and distribution. This on-module power management improves power efficiency while reducing vulnerability to power noise on the motherboard — a critical advantage for high-density server deployments where multiple DIMMs operate in close proximity. One PMIC is present on each DDR5 module.

EXHIBIT 14: **Upgrading to DDR5 introduces an on-module PMIC, which improves power efficiency while reducing vulnerability to power noise on the motherboard**



Source: Samsung, Bernstein analysis

PC DDR MODULE FORMATS AND CKD

While this report mainly focuses on server memory interface chips, the parallel developments in PC and laptop DDR modules represent an incremental — though structurally smaller — TAM opportunity.

PC and laptop memory uses two primary formats: SODIMM (laptops) and UDIMM (desktops). Unlike server RDIMMs and MRDIMMs, these modules do not employ RCD or data buffer chips, while the CPU memory controller communicates directly with DRAM without intermediary buffering. As a result, DDR4-generation PC modules contained essentially no on-module chipsets.

DDR5 changes this picture. Beyond the SPD Hub and PMIC now standard across all DDR5 formats, JEDEC has defined a new chip specifically for PC memory: the **CKD (Clock Driver)**. The CKD buffers and re-drives clock signals on DDR5 UDIMM and SODIMM modules, enabling stable operation at 6400 MT/s and above, speeds at which the unbuffered architecture would otherwise suffer from signal degradation. One CKD is required per module. Montage was the first vendor to deliver a CKD chip for sampling in September 2022. The CKD is distinct from the server-side RCD/MRCD. CKD buffers only clock signals, carries a lower ASP, and is not paired with data buffers. It therefore represents a complementary product category that expands the TAM into PC memory for the first time, albeit at a fraction of the server opportunity. One headwind to monitor is the rapid adoption of LPDDR in laptops, which is soldered directly without DIMM modules and will limit SODIMM-based CKD volume over time.

EXHIBIT 15: **Apart from DDR formats for servers, SODIMMs and UDIMMs are DDR modules for PC, introducing CKD in DDR5 era**

Main application	DIMM type	Memory interface chips	Product sample
Laptop	SODIMMs (small outline DIMMs)	DDR3 and DDR4: No DDR5: 1 unit of CKD, 1 unit of PMIC, 1 unit of SPD	
Desktop	UDIMMs (unbuffered DIMMs)	DDR3 and DDR4: No DDR5: 1 unit of CKD, 1 unit of SPD	
Server	RDIMMs (registered DIMMs)	DDR3 and DDR4: 1 unit of RCD DDR5: 1 unit of RCD, PMIC + SPD + 2 units of TS	
Server	LRDIMMs and MRDIMMs	DDR4 LRDIMM: 1 unit of RCD + 9 units of DB DDR5 MRDIMM: 1 unit of MRCD + 10 units of MDB, PMIC + SPD + 2 units of TS	

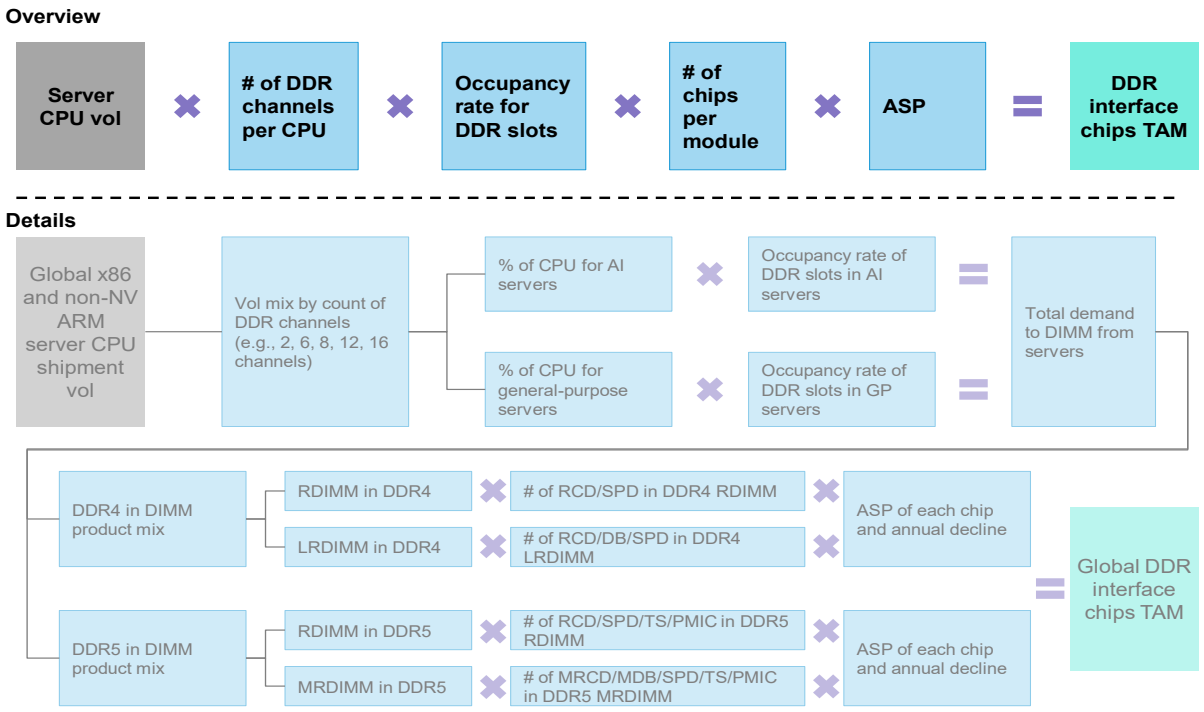
Source: Micron, Bernstein analysis

TAM SIZING AND ANALYSIS ON GROWTH DRIVERS

We project the global DDR module chipset TAM to reach USD 20Bn by 2030 (~65% CAGR '25–'30, Exhibit 3), significantly outpacing server CPU shipment growth (~24% CAGR '25–'30). This divergence reflects a structural dynamic: nearly all multiplicative factors in the TAM formula are rising simultaneously. The memory wall has become the performance bottleneck in AI clusters, accelerating memory technology upgrades and positioning memory interface chips in an increasingly vital role within the server architecture.

By 2030, MRDIMM-related chips (MRCD and MDB) are projected to account for approximately 73% of the total memory interface chip TAM, a category that barely existed before 2025. This concentration underscores the transformative impact of the MRDIMM migration on the industry's revenue pool.

EXHIBIT 16: **Our TAM model follows a bottom-up approach, reflecting the impacts of three drivers on five multiplicative factors**



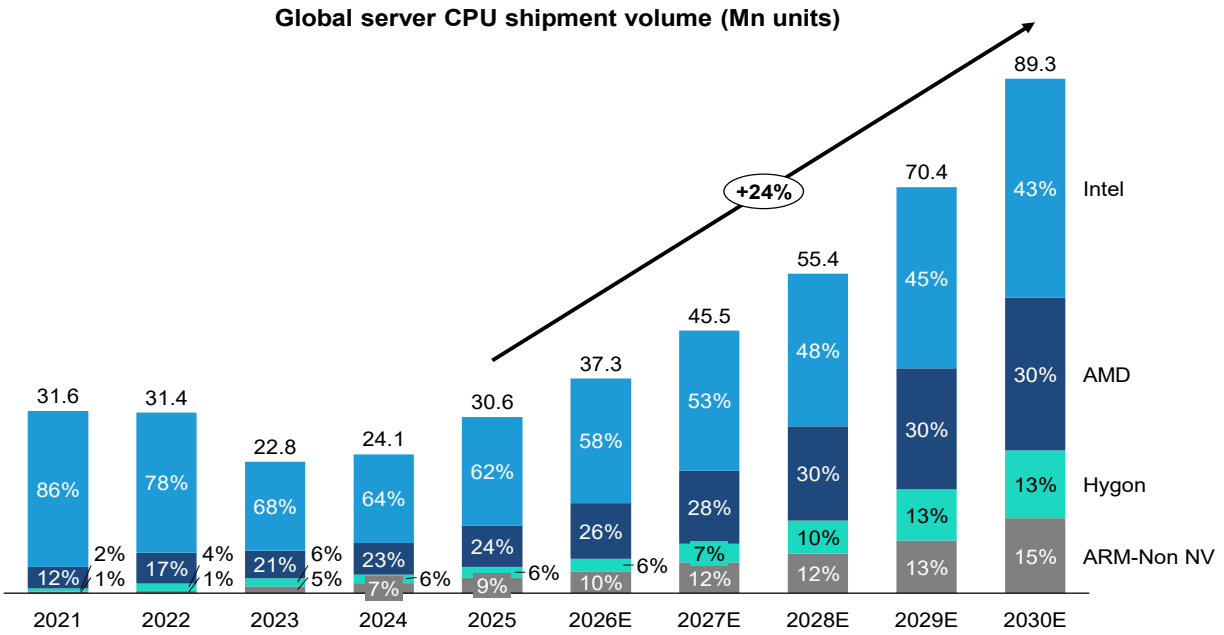
Source: Bernstein analysis

INCREASING SERVER CPU SHIPMENTS

We project global server CPU shipment volumes (excluding NVIDIA's proprietary CPUs) to grow from approximately 30.6 million units in 2025 to 89.3 million units by 2030, representing an 24% CAGR over the period. This growth is driven by the rapid expansion of AI server deployments, which require CPUs alongside GPU/accelerator arrays, as well as the continued build-out of cloud and enterprise infrastructure.

Within this total, AI server CPUs are growing significantly faster than general-purpose server CPUs. As NVIDIA shifts its proprietary CPUs (Grace) to LPDDR — which does not require the same DIMM chipset — DDR memory interface chip demand becomes primarily tied to x86 and non-NVIDIA ARM CPU shipment volumes.

EXHIBIT 17: **Faster CPU volume growth should translate directly into stronger demand for memory interface chips**



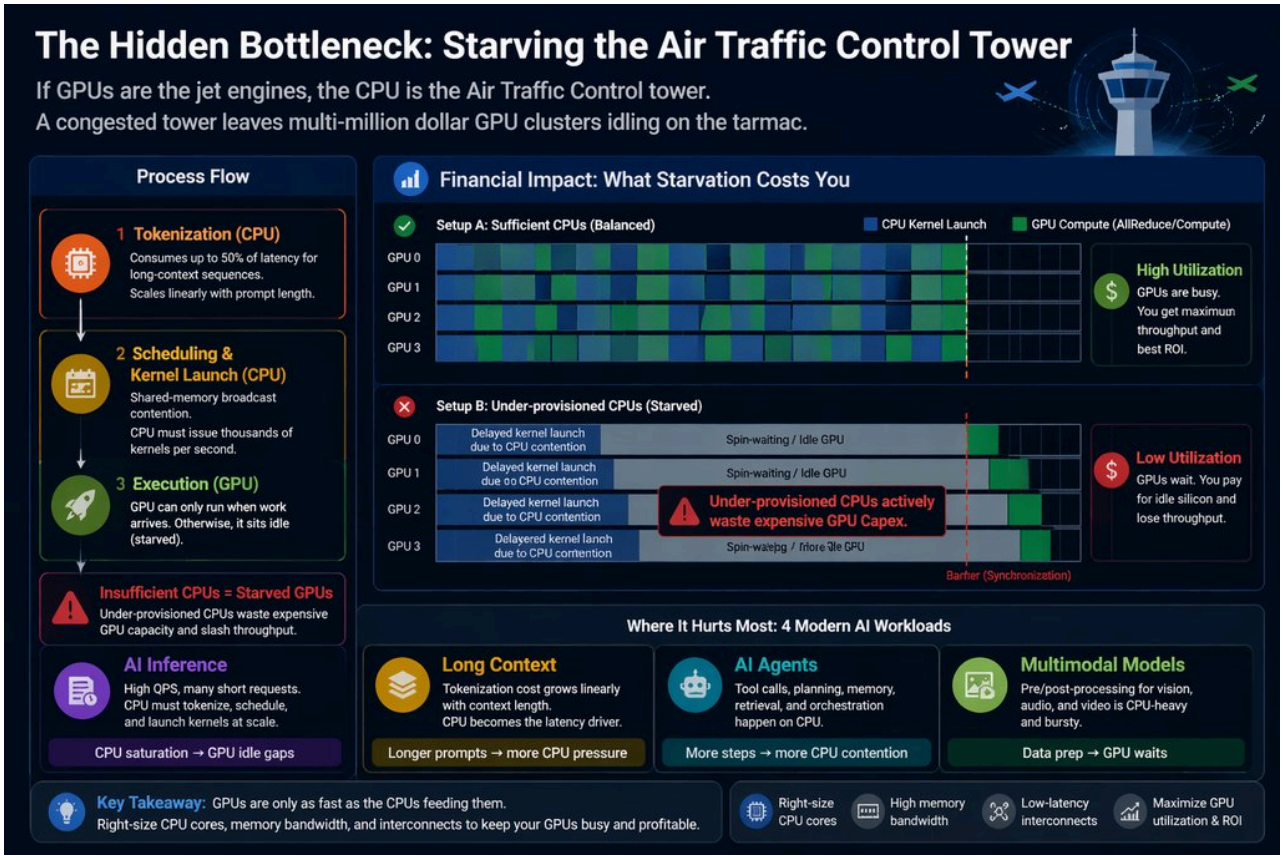
+ As NVIDIA CPUs shift to LPDDR, it requires only voltage regulators and PMIC. Our TAM projection of DDR memory interface chips is primarily tied to x86 and non-NV ARM CPU shipment volumes.

Source: Mercury Research, Bernstein analysis and estimates

Our global server CPU shipment volumes upward revision is driven by the convergence of AI agents, long-context processing, and multimodal models that push CPU utilization higher.

The economic implications are compelling. Research from Georgia Tech has demonstrated that CPU under-provisioning in multi-GPU LLM inference clusters can increase time-to-first-token by 1.4× to 5.4×, effectively leaving multi-million-dollar GPU clusters idling on the tarmac. Yet CPU cores are approximately 100–1,600× cheaper than equivalent GPU compute, meaning that increasing the CPU allocation typically adds only about 1.5% to total cluster cost while potentially unlocking dramatically higher GPU utilization. This creates a strong economic incentive for CSPs to aggressively increase CPU provisioning — a trend that directly drives DDR module chipset demand, since every additional CPU requires multiple DDR modules, each populated with module chipsets.

EXHIBIT 18: **CPU under-provisioning leaves GPUs idle. Adding CPU cores is cost-effective to improve performance. Because CPU cores are approximately 100–1,600x cheaper than GPU compute, increasing the CPU allocation typically adds only about 1.5% to the total cost while potentially improving time-to-first-token by 1.36–5.40x**



Source: Chung, Euijun, et al. "Characterizing CPU-Induced Slowdowns in Multi-GPU LLM Inference." Georgia Tech, 2026; Bernstein analysis

Beyond DDR, the CPU Renaissance is also structurally favorable for CXL-based memory expansion. AI agents require massive persistent memory for KV cache and context windows, and CPUs provisioned with large, disaggregated RAM pools via CXL memory pooling offer a more efficient architecture for accommodating the growing data volumes generated by long task chains — compared to HBM bound directly to GPUs. We view the CPU Renaissance as a material upside catalyst not yet reflected in either our estimates or Street consensus, and one that investors should monitor closely as agentic AI deployments scale through 2027–2030.

RISING DIMM MODULES PER CPU

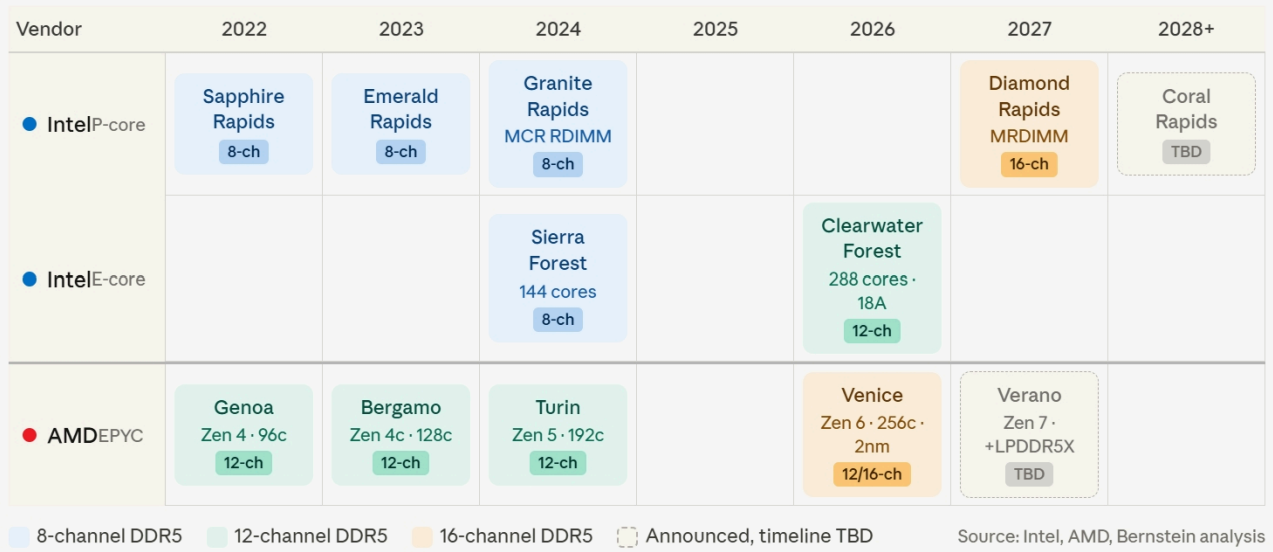
The second growth driver is the increasing number of DDR modules per CPU, which is a function of two sub-drivers: the migration to higher channel-count CPU architectures and the rising occupancy rate of DIMM slots.

Channel count migration: The number of DDR channels per CPU is migrating upward in response to AI workloads that are extremely bandwidth-hungry. The share of server CPUs with 12-channel DDR configurations will grow from 24% in 2025 to 45% in 2030, while 16-channel CPUs will rise from near zero to 30% over the same period. This transition has the potential to roughly double the memory interface content required per CPU.

The drivers behind this migration are clear. AI workloads demand massive memory bandwidth, since additional channels reduce contention and latency during parallel computing. CPU core counts are scaling faster than per-DIMM bandwidth, meaning that adding channels is necessary to sustain bandwidth per core and avoid memory starvation. Higher channel counts also enable more DIMM slots and greater total memory capacity per socket, supporting virtualization density, LLM inference, and large memory-resident workloads.

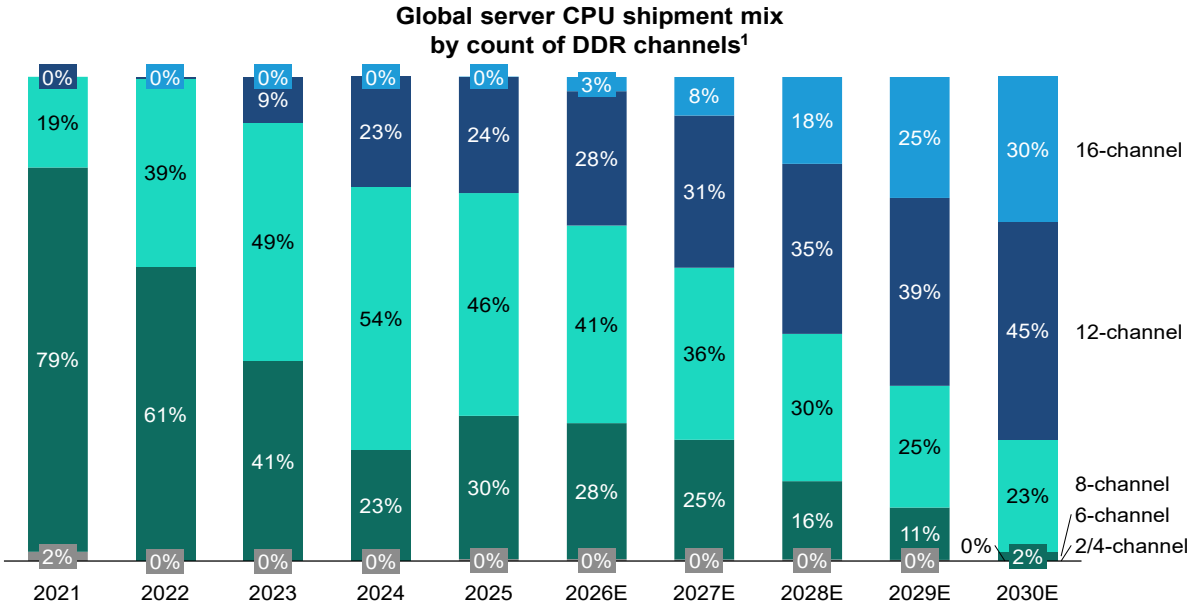
Competition between Intel and AMD to raise the bar on DDR channel count ensures that neither vendor can afford to fall behind on memory specifications, creating a secular ratchet effect. Intel's Sapphire Rapids and Emerald Rapids (2023–2024) operated on 8-channel DDR5 architectures. The step-change comes with Clearwater Forest (1H 2026), Intel's next-generation E-core platform, which doubles the channel count to 12-channel DDR5 with up to 288 cores. Looking further ahead, Diamond Rapids, Intel's next P-core platform (expected in mid-2027), is designed with 16-channel DDR5 support. On the AMD side, the channel count migration began earlier. AMD's Genoa (EPYC 9004, 2022) debuted with 12-channel DDR5. The upcoming Venice (EPYC 9006, 2026), built on Zen 6 architecture with TSMC 2nm and up to 256 cores, is expected to support up to 16 channels of DDR5 on the new SP7 socket.

EXHIBIT 19: **The competitive dynamic is self-reinforcing: neither Intel nor AMD can afford to lag on memory bandwidth specs. The migration to 12- and 16-channel architectures will proceed on schedule or even accelerate**



Diamond Rapids reportedly delayed to mid-2027. Venice SP7 platform supports both 12-ch and 16-ch DDR5 configurations with RDIMM and MRDIMM. Verano adds LPDDR5X SOCAMM2 support alongside DDR5. Both Intel and AMD also support MRDIMM from their respective platforms.
Source: Intel, AMD, Bernstein analysis

EXHIBIT 20: **The transition from 8-channel to 16-channel DDR architectures has potential to double memory interface content required per CPU**



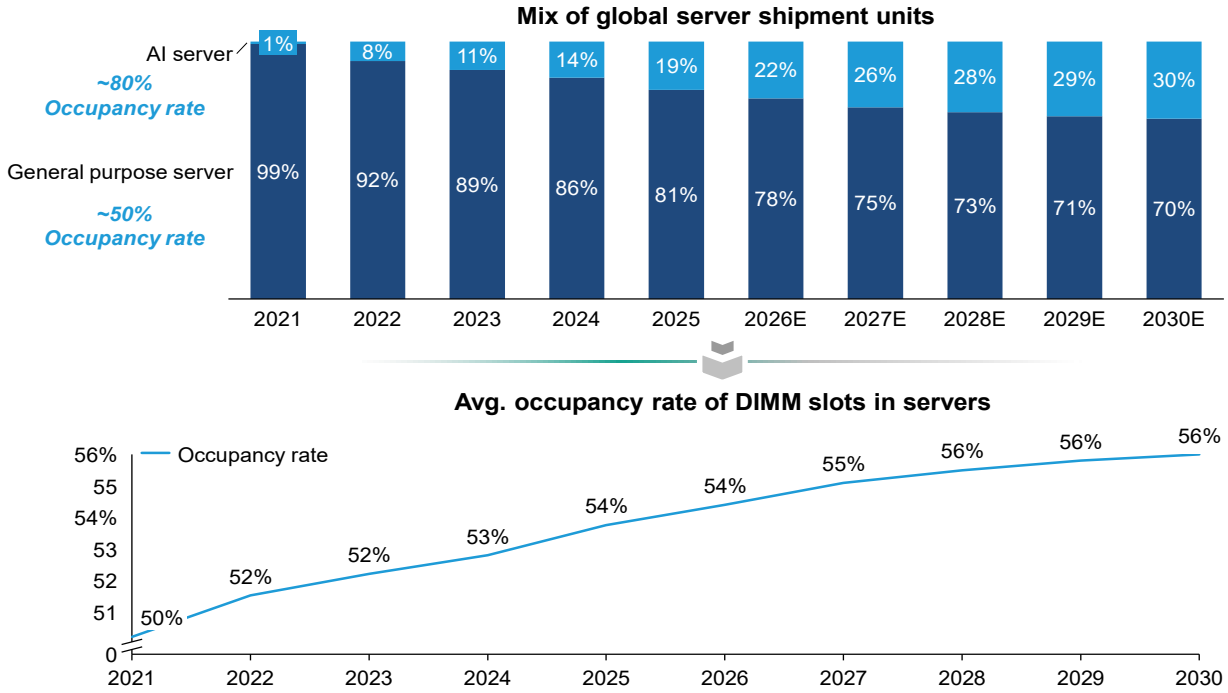
CPUs are categorized based on the higher DDR-channel count available among their versions (e.g., Clearwater Forest's 8-channel and 12-channel variants are grouped under 12-channel). In the explicit model, we instead use the weighted average DDR-channel count.
Source: Mercury Research, Bernstein analysis and estimates

Occupancy rate increase: AI servers fully populate DDR slots with approximately 70-80% occupancy to optimize accelerator utilization. The logic is straightforward: insufficient DDR capacity directly caps xPU utilization, and with accelerators representing the majority of the system BOM cost, maximizing xPU utilization far outweighs the incremental cost of populating every memory slot. Larger DDR capacity with manageable bandwidth trade-offs (losing 5–15%) is acceptable in AI's parallel compute profile, and symmetric DDR configurations are critical for scale-up AI systems.

By contrast, general-purpose servers leave roughly half of memory slots empty (~50% occupancy) to optimize fleet-level TCO and preserve headroom for future upgrades. DRAM accounts for approximately 50% of GP server CAPEX and is energy-intensive, making overprovisioning costly. GP servers expand via scale-out, with half-populated slots preserving flexibility to upgrade memory and add servers as needed.

As AI servers grow from approximately 14% of global server shipments in 2024 to an estimated 30% by 2030, the blended average occupancy rate of DIMM slots across the global server fleet rises from approximately 54% to 56% — a meaningful uplift in total DIMM demand per CPU shipped.

EXHIBIT 21: **AI servers utilize nearly all DIMM slots to maximize accelerator performance, while traditional servers prioritize TCO and leave many slots unpopulated. The shift toward AI servers will drive higher average DIMM slot occupancy**



Source: Gartner, Bernstein analysis and estimates

HIGHER MEMORY INTERFACE CHIPS VALUE PER MODULE FROM MRDIMM MIGRATION

The migration from DDR4 to DDR5, and subsequently from DDR5 RDIMM to DDR5 MRDIMM, is a powerful driver of dollar content per package expansion for memory interface chips. DDR5 modules require additional chip types beyond the RCD and SPD that were only interface chips in DDR4 RDIMM; specifically, PMIC and TS are now integrated, lifting the total interface chip count per RDIMM module. More importantly, the transition to MRDIMM represents a step-change in silicon content: each MRDIMM module adopts a "1+10" architecture consisting of one MRCD chip and ten MDB chips, compared to one RCD and zero data buffers for a DDR5 RDIMM at 6400MT/s. This translates to a dramatic increase in memory interface silicon content per module, directly boosting Montage's dollar content per DIMM sold. We estimated that the memory interface chip total value could increased from about 7 USD in RDIMM to more than 70 USD in MRDIMM (with all interface chip combined).

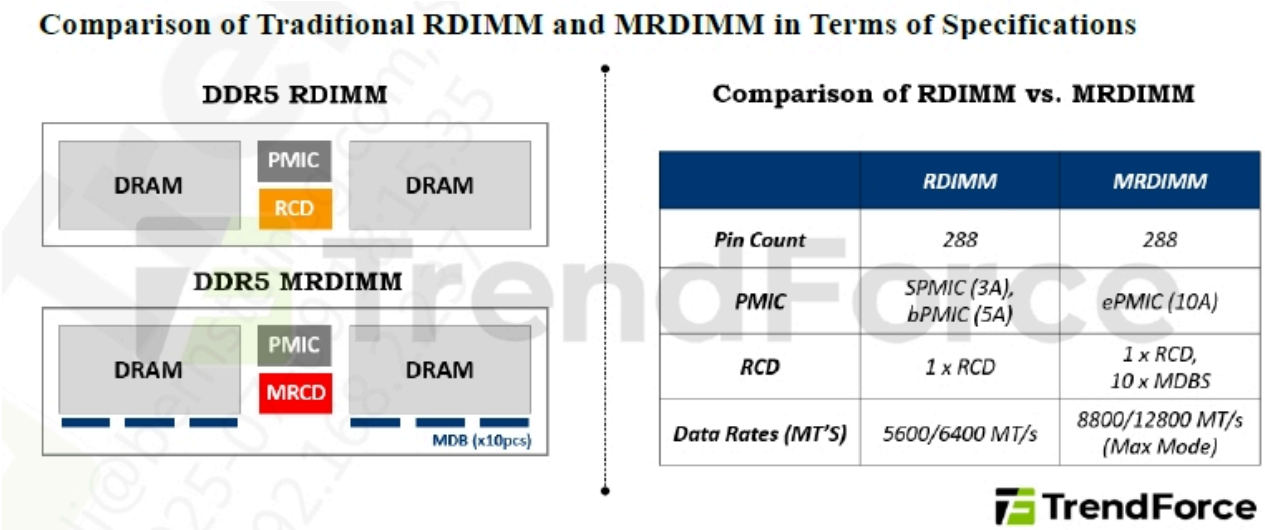
As a result, MRDIMM penetration is the single most sensitive variable in the TAM model. TrendForce estimates MRDIMM just accounts for 3% of global server DDR DIMM shipment units in 2026; and we project the rate will rise to 25% by 2030E.

CONFIGURATION COMPARISON ACROSS DDR GENERATIONS AND DIMM FORMATS

The chip count and composition per module varies significantly across DDR generations and DIMM formats, with each upgrade cycle introducing additional silicon content.

The key takeaway from the comparison across module formats in Exhibit 23 is the dramatic step-change in silicon content when moving from DDR5 RDIMM to DDR5 MRDIMM. MRDIMM adopts a "1+10" architecture (one MRCD plus ten MDB chips) versus just one RCD and zero data buffers for DDR5 RDIMM at 6400 MT/s. The total DDR chipset value amplifies by approximately 10 times for MRDIMM versus RDIMM: from roughly USD 7 in total interface chip value per RDIMM module to more than USD 70 per MRDIMM module (with all interface chips combined). This step-change is the single most important structural driver of TAM expansion.

EXHIBIT 22: **The spec upgrade of MRDIMM versus RDIMM**



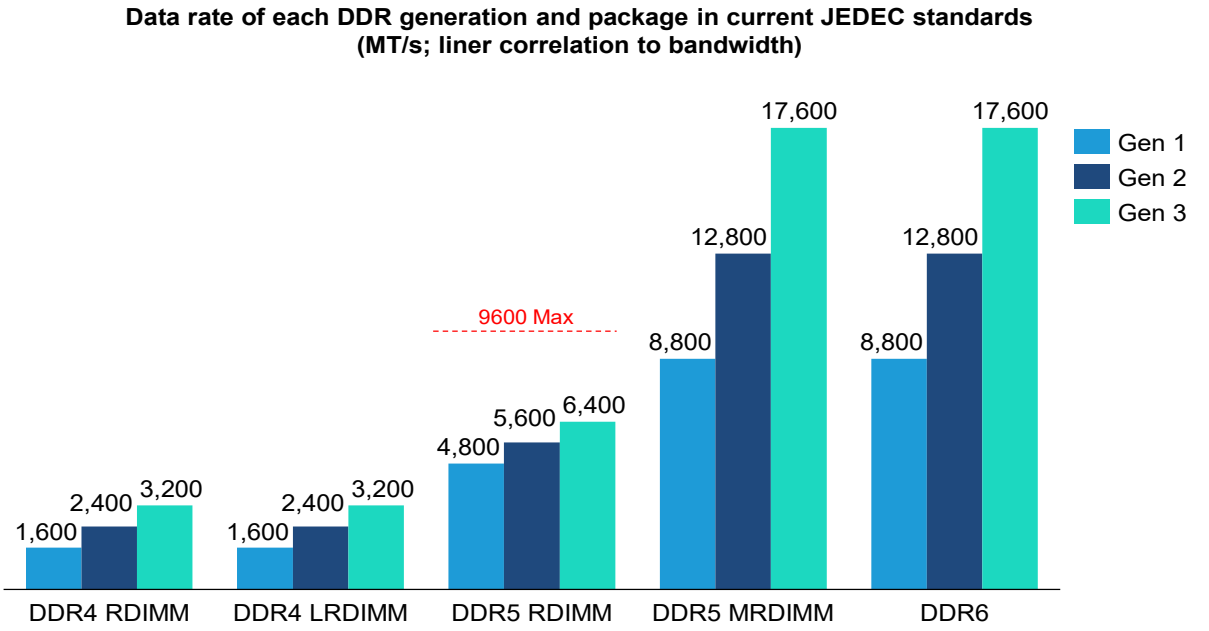
Source: TrendForce report in 2025 July

EXHIBIT 23: **Memory interface chips configuration comparison across various formats of server DDR4 and DDR5**

Unit of chips	DDR4 RDIMM	DDR4 LRDIMM	DDR5 RDIMM	DDR5 MRDIMM
RCD	1	1	1	
DB		9		
MRCD				1
MDB				10
SPD	0 or 1	0 or 1	1	1
TS			2	2
PMIC			1	1
ASP of the whole memory interface chipset	USD 2-3	USD 12-14	USD 6-7	USD 70-80

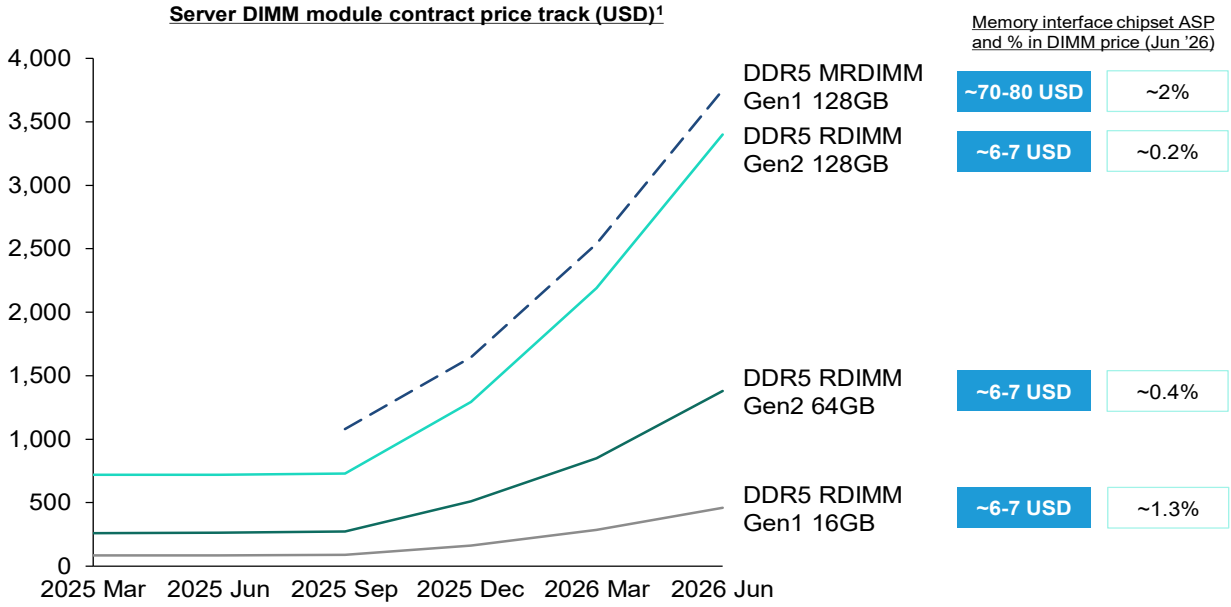
This chart shows our estimation of the chip price in 2026, we expect the price to further drop in the next few years.
Source: Montage reports, Bernstein analysis

EXHIBIT 24: **DDR5 MRDIMM achieves DDR6-class data rates while leveraging the existing DDR5 physical architecture. This capability underpins our confidence in the strong adoption of MRDIMM**



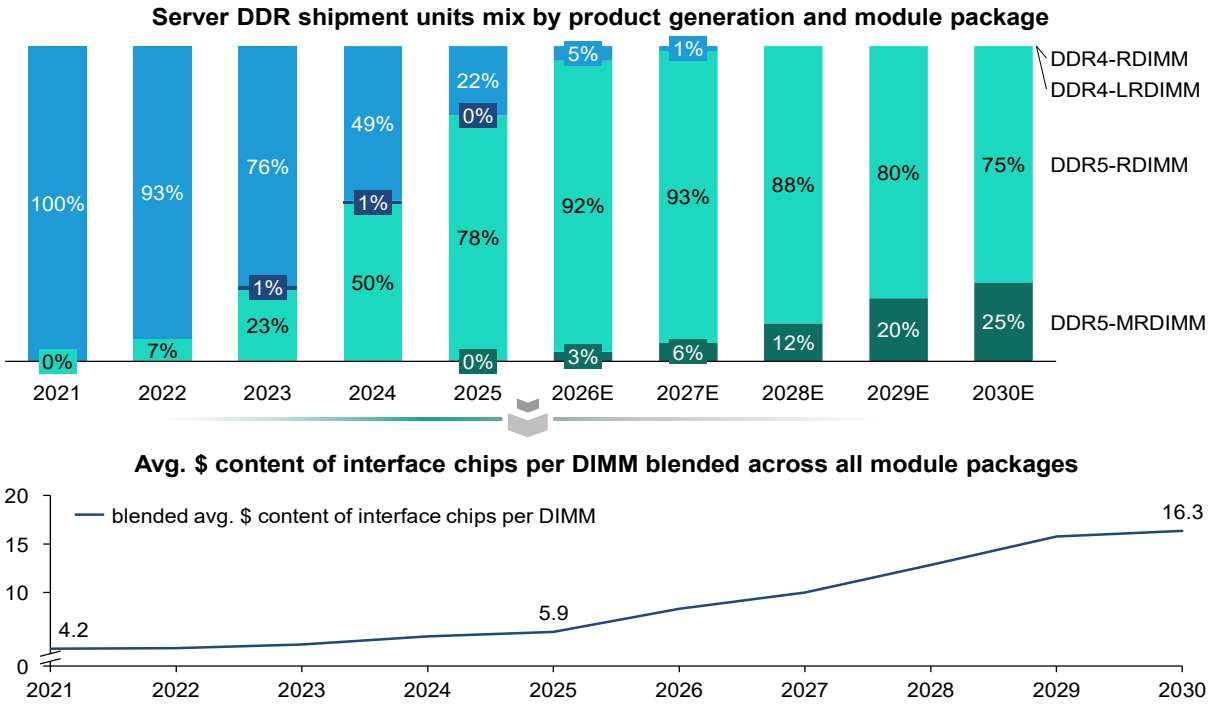
Source: JEDEC, Bernstein analysis

EXHIBIT 25: **Memory interface chips account for only an LSD portion of module costs, limiting pricing pressure. Rising memory prices are also reducing MRDIMM's premium over RDIMM to around 10%, reducing adoption barriers of MRDIMM**



MRDIMM remains a niche product without an established contract pricing track record. The MRDIMM pricing shown in the chart is an estimate based on public information; in general, we estimate MRDIMM enjoys a $300-350 markup over RDIMM at the same capacity
Source: TrendForce, Bernstein analysis and estimates

EXHIBIT 26: **MRDIMM adoption in the DDR5 era will nearly triple memory interface chips dollar content per module. We expect MRDIMM penetration to surpass 25% by 2030, a level that remains modest compared with the adoption trajectory of DDR5 RDIMMs**



Source: TrendForce, Bernstein analysis and estimates

Why do we believe the MRDIMM adoption will accelerate?

- **First, data rates above 8800 MT/s exceed RDIMM's practical signal integrity limits**. Without active retiming, RDIMM faces crosstalk and signal loss at high data rates — a fundamental physical constraint that cannot be solved through incremental improvements to passive architectures. MRDIMM's MRCD and MDB actively reshape and re-clock signals on the module, maintaining integrity at 8800–12800 MT/s.

- **Second, CPU platform support is broadening**. Intel committed to MRDIMM support from its first-generation DDR5 MRDIMM-compatible platform, and AMD has followed by supporting MRDIMM from its second generation. It signals to the entire downstream ecosystem that the format will see sustained investment and qualification.

- **Third, the memory supercycle helps close the cost gap**. As DRAM die prices rise, the interface chipset becomes a proportionally smaller component of total module cost, compressing the percentage cost gap between RDIMM and MRDIMM, which incentivizes CSPs to shift from RDIMM to MRDIMM faster.

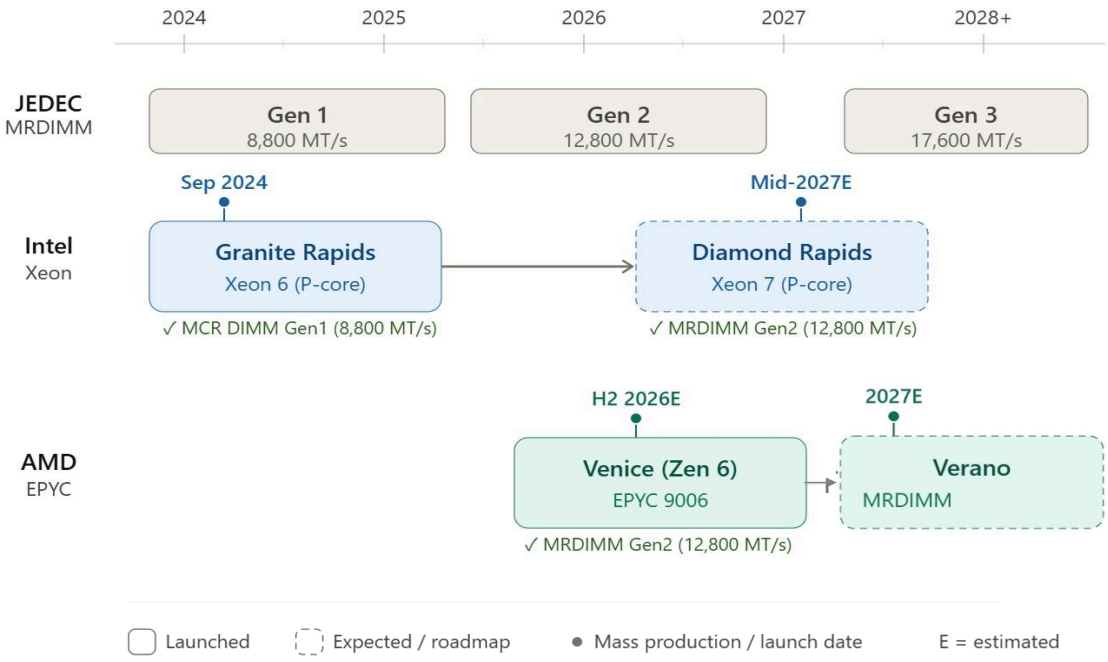
Why will MRDIMM not repeat LRDIMM's failure?

The most common bear-case objection: DDR4 LRDIMM also carried high interface chip content yet never exceeded 1% of server DDR shipments. Why should MRDIMM be different? We see structural differences:

- **LRDIMM solved the wrong problem.** LRDIMM offered higher capacity without improving bandwidth, as the data buffers added latency while per-module bandwidth stayed flat. In the DDR4 era, capacity was not the binding constraint. MRDIMM addresses both dimensions: its multiplexed architecture doubles per-module bandwidth while also supporting higher capacity, directly tackling the bandwidth bottleneck that AI workloads create.

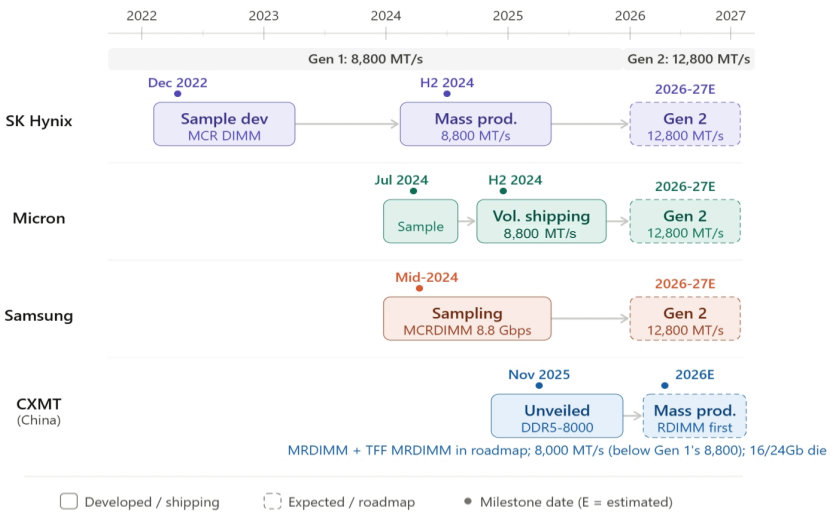
- **RDIMM was "good enough" in DDR4; it is not in DDR5.** RDIMM handled DDR4 data rates (up to 3200 MT/s) without signal integrity issues, giving customers no reason to migrate. At DDR5 speeds of 8800 MT/s and above, RDIMM can no longer maintain clean signals. The migration to MRDIMM is pulled by physics, not pushed by marketing.
- **Platform commitment versus orphan status.** Neither Intel nor AMD published a Plan of Record for DDR5 LRDIMM, effectively killing the format. MRDIMM has explicit support from both vendors.
- **AI servers create a customer base that did not exist.** DDR4-era servers were predominantly general-purpose machines with moderate memory needs. AI servers fully populate DIMM slots and push every specification to the limit; hence, they are the natural high-volume customer base for a format that delivers maximum bandwidth.
- **The memory supercycle narrows the cost gap.**

EXHIBIT 27: **Intel led the migration to MRDIMM with Granite Rapids in 2H24, while AMD enters directly to MRDIMM Gen2 in 2026, with Venice as the first MRDIMM-capable platform**



Source: Intel and AMD reports, Bernstein analysis

EXHIBIT 28: **DRAM suppliers have established solid MRDIMM product roadmaps; notably, CXMT is rapidly catching up with global leaders**



Source: SK Hynix, Samsung, Micron, CXMT reports, Bernstein analysis

COMPETITIVE DYNAMICS AND INDUSTRY MOAT

The core memory interface chip market is a textbook oligopoly with ~92% share held by three players. High barriers to entry protect incumbents, including JEDEC certification, multi-party validation, and advanced node fabrication. The complementary chip market is more fragmented, with many conventional analog or sensor suppliers.

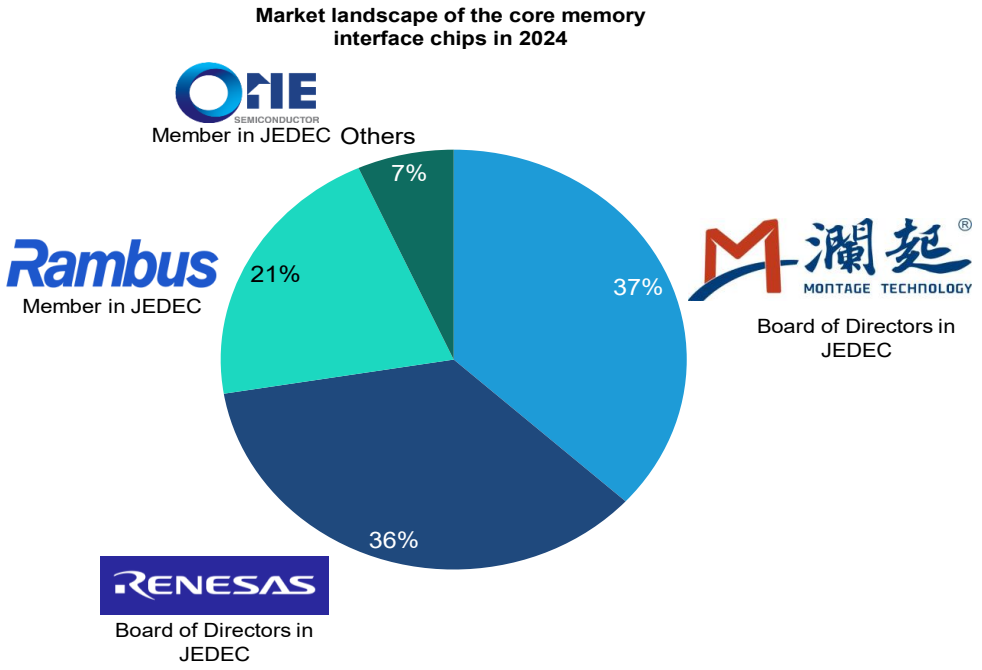
CORE MEMORY INTERFACE CHIPS MARKET: A CONSOLIDATED OLIGOPOLY

The core memory interface chip market exhibits a degree of concentration that is unusual even by semiconductor industry standards. Three players — Montage Technology (~37% market share), Renesas (~36%), and Rambus (~20%) — collectively controlled approximately 92% of global market share by revenue as of 2024. The only other meaningful participant is One Semiconductor, a Korean company that has emerged as a small player offering RCD and CKD products, manufacturing on Samsung Foundry's process platform. One Semiconductor was founded by the former Head of DRAM Development at Samsung Electronics and the former Chief Technology Officer of Samsung Electro-Mechanics. Despite its close ties to Samsung, the company has struggled to meaningfully scale its market share, underscoring the exceptionally high technological and ecosystem barriers in this sector.

These structural barriers have progressively eliminated competitors across successive DDR generations, resulting in the current level of industry concentration. Compliance with JEDEC standards demands deep expertise in high-speed serial interface design, analog/mixed-signal engineering, and memory controller protocols. In addition, the multi-party qualification and validation process—spanning foundries (primarily TSMC), CPU vendors (Intel, AMD), JEDEC committee participation, DRAM manufacturers (Samsung, SK Hynix, Micron, CXMT), module vendors (e.g., Kingston), and OEMs/CSPs—typically requires 18–24 months from initial silicon to volume production approval. During this period, any design flaw or interoperability failure can fully disqualify a supplier.

RCD and MRCD are the most technically complex components among the DIMM chipset family, fabricated at leading-edge CMOS nodes. DDR4 RCDs were manufactured on 40nm platforms, while DDR5 first-generation RCDs started at 28nm. Future RCD and MRCD generations for DDR5 will offer faster data rates and could employ even more aggressive technology nodes (down to 10nm below class), raising the technological bar for any potential new entrant.

EXHIBIT 29: **The core memory interface chips market is a textbook oligopoly, with top 3 players consolidating 90+% of market share**



Source: company reports, Bernstein analysis and estimates

COMPLEMENTARY SUPPORTING CHIPS: A MORE FRAGMENTED MARKET

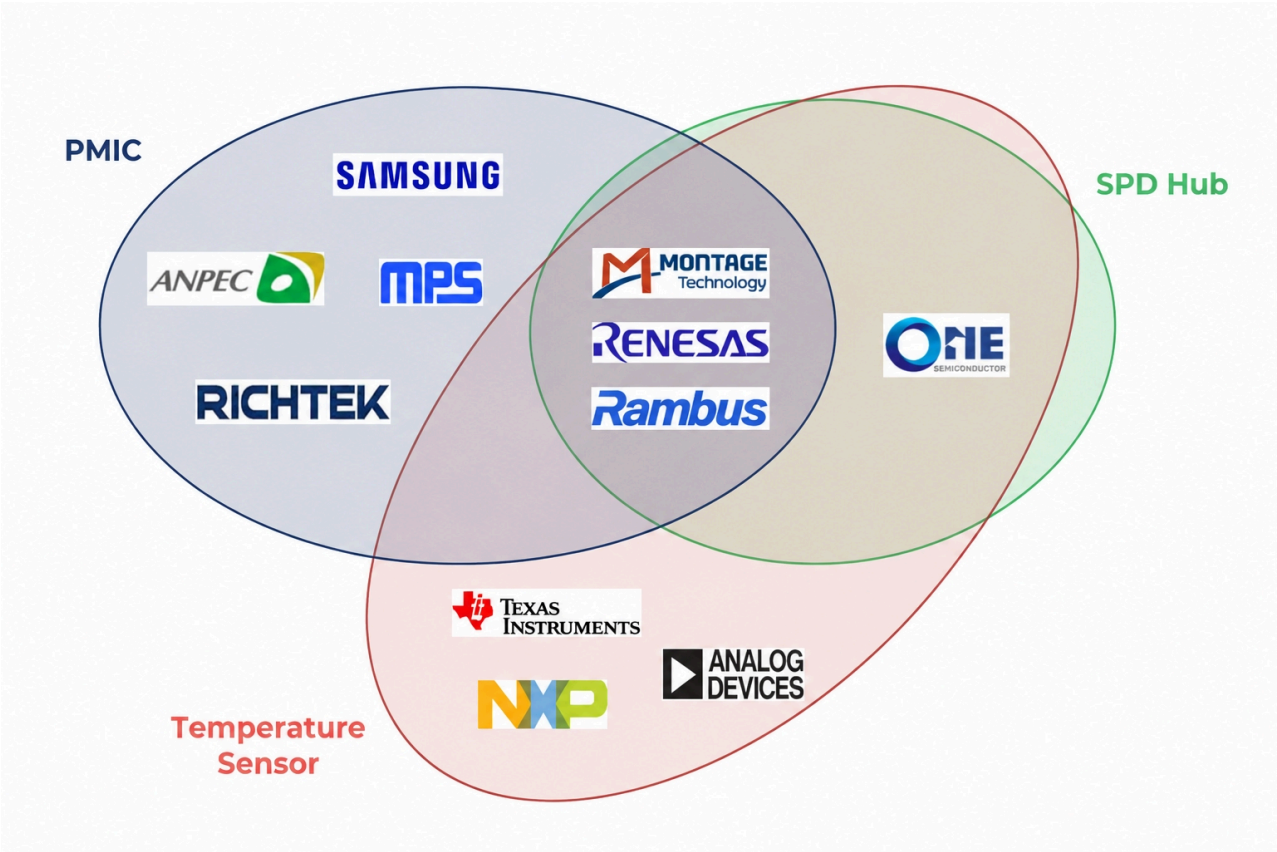
In contrast to the oligopolistic structure of the memory interface chip market, the complementary supporting chip market (PMIC, SPD Hub, TS) is considerably more fragmented, with dozens of analog and discrete IC vendors participating. The technical barriers are relatively lower: these components do not require the same level of high-speed digital design expertise as RCDs, and they are fabricated on mature process nodes rather than leading-edge CMOS.

Renesas is the market leader in complementary chips with the largest market share of DDR5 PMIC/SPD/TS, leveraging the deep analog product expertise it acquired through its 2019 acquisition of Integrated Device Technology (IDT) for $6.7 billion. IDT had been the market leader in DIMM chipsets prior to the acquisition, and Renesas used the deal to reinforce its position in advanced communications and automotive mixed-signal products.

Montage achieved portfolio completeness at DDR5 launch in October 2021, but partly through manufacturing partners: Giantec Semiconductor (Shanghai) for SPD Hub and Global Mixed-mode Technology (Taiwan) for PMIC. This preserved R&D focus on core RCD/DB competency. More recently, Montage appears to be building in-house PMIC and SPD design capability, with its US office now recruiting analog engineers for these products.
Rambus initially lacked complementary chips, a noted disadvantage; but it closed the gap through sequential in-house development: SPD Hub and TS in July 2022, server PMICs in April 2024, and the PMIC5030 for MRDIMM in October 2024.

Other notable participants in the complementary chip space include Samsung, Monolithic Power Systems, Richtek, Texas Instruments, NXP, and Analog Devices. The lower barriers and higher number of participants mean that pricing power in complementary chips is significantly weaker than in memory interface chips.

EXHIBIT 30: **Besides the three leading players with full chipsets, a range of analog and discrete suppliers also provide complementary supporting chips**



Source: Yole, Bernstein analysis

EVALUATION OF THREE CORE MEMORY INTERFACE CHIP PLAYERS

Montage, Renesas, and Rambus collectively controlled over 90% of global core memory interface chips market share in 2024. Barriers to entry are formidable: chips must pass 18–24 month qualification cycles with DRAM vendors, CPU platform providers, and CSPs, while incumbents shape the JEDEC specifications that new entrants must meet. Suppliers who fall behind a DDR generation have historically been eliminated. We evaluate the three players across product portfolio breadth, DDR5 RDIMM roadmap, and MRDIMM positioning.

Product portfolio breadth: all three now offer complete DDR5 chipsets, but through different paths

DDR5's expanded module architecture introduced PMIC, SPD Hub, and Temperature Sensor alongside the traditional RCD and DB, making a complete chipset offering a competitive imperative for module manufacturers seeking one-stop sourcing.

Renesas entered DDR5 with the broadest in-house portfolio from the outset, inheriting deep analog and power management expertise through its 2019 acquisition of IDT (USD 6.7Bn), which had launched the industry's first DDR5 PMIC in 2017 and held the largest PMIC share among the three incumbents.

Montage achieved portfolio completeness through manufacturing partnership at the beginning, but is gradually building up in-house design capabilities for complementary supporting chips.

Rambus initially lacked complementary chips, but has closed the gap through sequential in-house development since 2022. With this build-out complete, Rambus now offers a fully in-house chipset for both RDIMM and MRDIMM.

In short, portfolio breadth is no longer a differentiator. The remaining distinction lies in the development model: Renesas leads on in-house analog heritage, Rambus has caught up through organic investment, and Montage bridges the gap through a hybrid

of partner-sourced and increasingly in-house capabilities.

DDR5 RDIMM roadmap: Renesas leads, Montage and Rambus in close pursuit

Renesas is slightly ahead, having reached mass production of DDR5 Gen 5 (8800 MT/s) and begun sampling Gen 6 (9600 MT/s) in November 2025.

Montage achieved mass production of Gen 4 (7200 MT/s) in October 2025 and is sampling Gen 5 (8000 MT/s), with Gen 6 still in R&D.

Rambus reached mass production of Gen 5 (8000 MT/s) in October 2024 but has not disclosed a Gen 6 timeline.

In practice, the commercial impact of Renesas's speed-grade lead is moderated by server platform qualification cycles, which tend to compress vendor timing within each platform launch window.

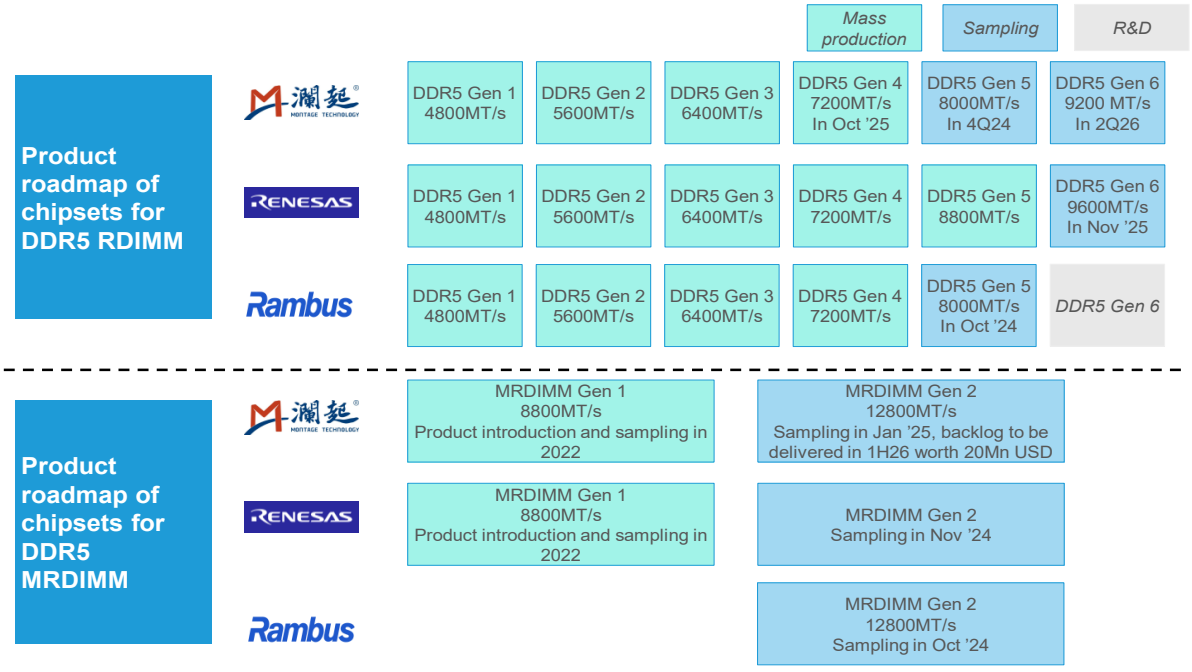
DDR5 MRDIMM chipsets: Montage and Renesas co-pioneered Gen 1; Rambus pivots directly to Gen 2

MRDIMM carries the highest-growth potential given the step-change in silicon content per module, making competitive positioning here disproportionately important for long-term share dynamics.

Both Montage and Renesas introduced Gen 1 MRDIMM chipsets (8800 MT/s) in 2022 on comparable timelines, establishing them as co-equal early movers. Their chipsets enabled the initial MRDIMM modules that shipped with Intel Granite Rapids in H2 2024. Rambus made a deliberate decision to skip Gen 1 entirely and direct resources toward Gen 2, after JEDEC formally unveiled the product standard.

For MRDIMM Gen 2 (12800 MT/s), the competitive landscape is more evenly contested. All three incumbents are now actively competing for Gen 2 design-ins, and ultimate share will depend on qualification outcomes, volume ramp execution, and pricing dynamics through 2026–2027.

EXHIBIT 31: **Three industry leaders remain closely matched in DDR5 RDIMM and MRDIMM offerings. However, Montage and Renesas hold a first-mover advantage in MRDIMM memory interface chips**



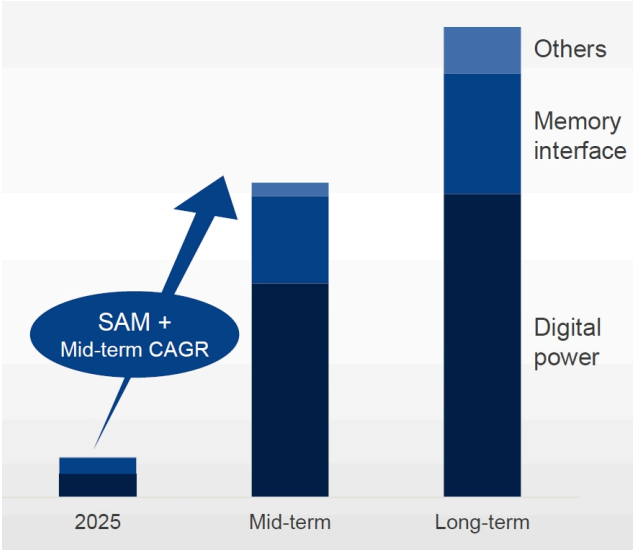
Source: companies official websites, Bernstein analysis

Renesas' Memory Interface Management Outlook Looks Conservative

Renesas's memory interface is at a scale similar to Montage's despite contributing only 6% of it revenue, yet its market cap is only 25% above Montage's; it appears significantly undervalued, and management's guidance for 20-30% growth CAGR for this business is too low.

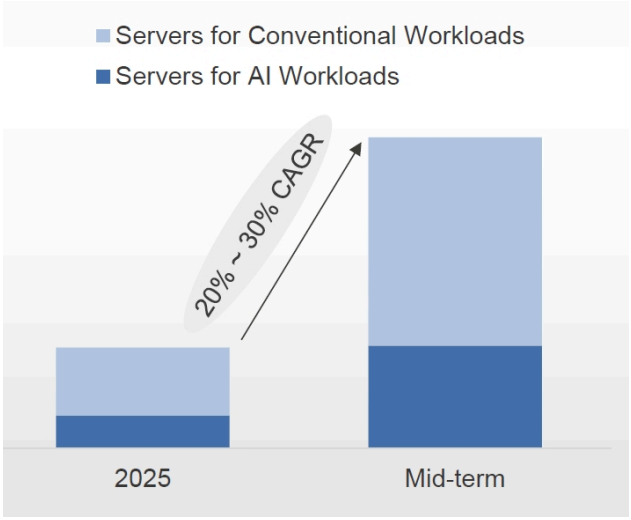
At Renesas' Capital Market Day (CMD) in June 2026 *(refer to Renesas CMD 2026: AI infra to drive revenue doubling)*, management guided for memory interface and other data-center-related revenue to grow at a 20-30% CAGR through 2030, vs. our TAM CAGR of 65% over 2025-2030 (Exhibit 32-Exhibit 33). We believe this outlook understates the opportunity. We forecast memory interface revenue to grow at a 42% CAGR over 2025-28, increasing from JPY84bn to JPY240bn and representing ~43% of AI infrastructure revenue by 2028 (Exhibit 34-Exhibit 35).

EXHIBIT 32: **Renesas' AI Infrastructure - Mid-to-Long Revenue Target**



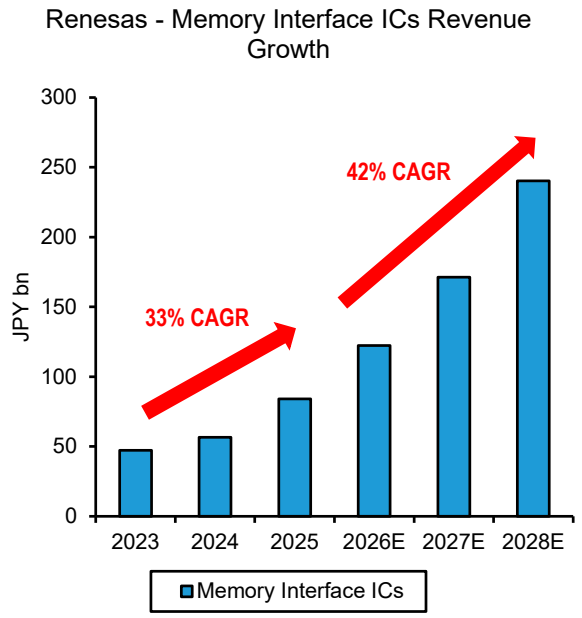
Source: Renesas

EXHIBIT 33: **Within AI infrastructure, Renesas' Memory Interface ICs' Mid-Term Revenue Target**



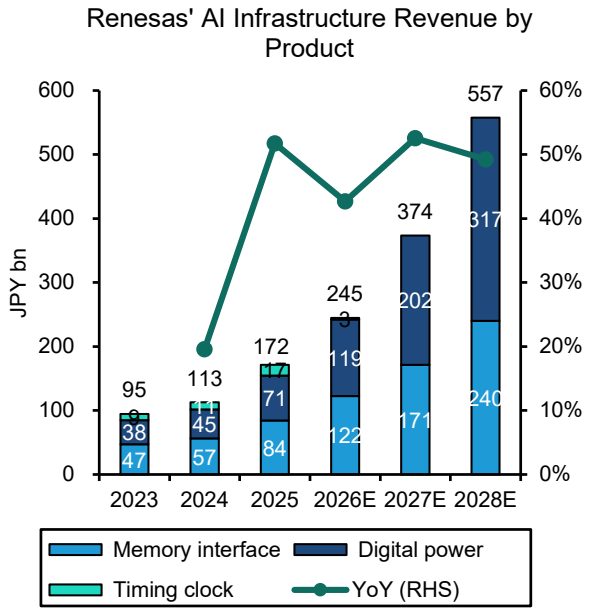
Source: Renesas

EXHIBIT 34: **Renesas - Memory Interface ICs Revenue Trend**



Source: Company disclosures, Bernstein estimates and analysis.

EXHIBIT 35: **Renesas' AI Infrastructure Revenue by Product**



Timing clock IC revenue is excluded from February 2026 onward following Renesas' divestiture of the business to SiTime (SITM, not covered), which closed in July 2026.
Source: Company disclosures, Bernstein estimates and analysis.

THE MOAT OF THE INDUSTRY

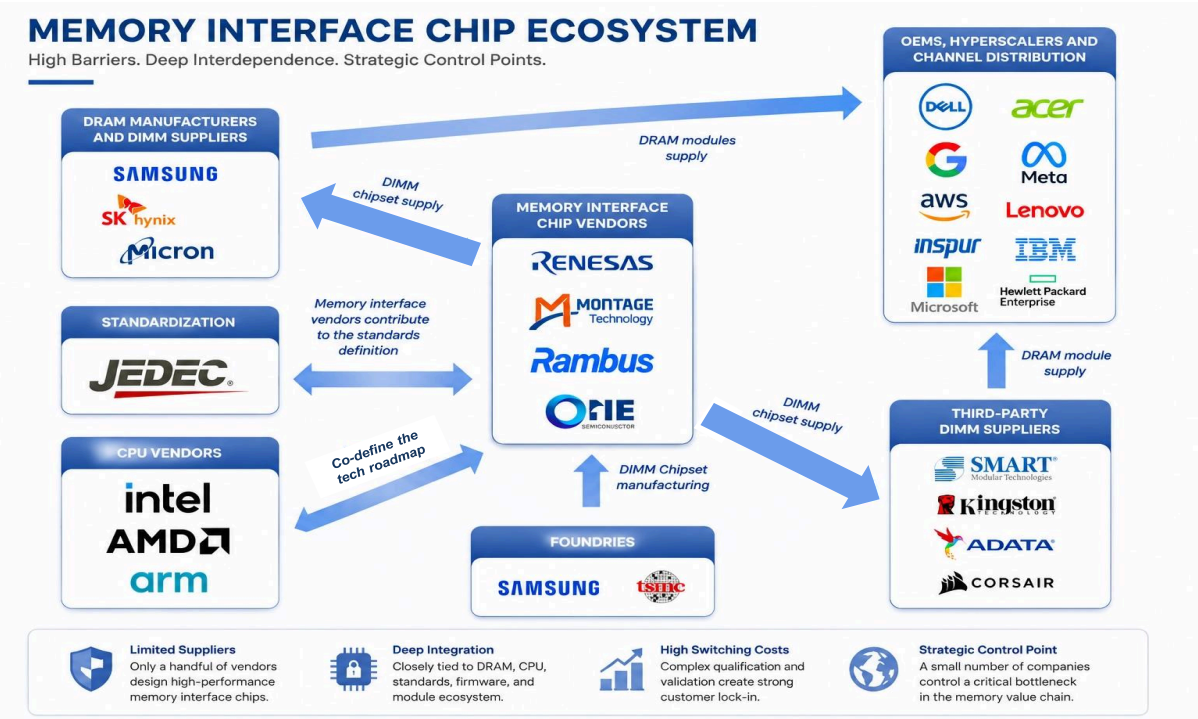
The memory interface chip market possesses deep structural moats, built on reinforcing pillars.

Standards definition through JEDEC participation: The three incumbent suppliers are all active members of JEDEC, the industry body responsible for defining DDR standards. Notably, Montage and Renesas sit on the JEDEC board of directors, granting them early visibility into upcoming specifications and the ability to influence standard setting. This creates a "roadmap definition" dynamic in which incumbents help shape the technical requirements that new entrants must ultimately meet—effectively defining the competitive landscape on their own terms.

Multi-party validation ecosystem and strong network effects: Bringing a new memory interface chip to market requires rigorous interoperability validation across a complex ecosystem, including foundries (primarily TSMC for advanced nodes), CPU vendors (Intel, AMD), JEDEC committees, DRAM manufacturers (Samsung, SK hynix, Micron, CXMT), module vendors (e.g., Kingston), and end customers such as OEMs and cloud service providers. This qualification process typically spans 18–24 months and must be repeated for each new product generation. For new entrants, this implies a minimum of 3–4 years from initial R&D investment to first meaningful revenue, assuming no qualification setbacks. The deeply interconnected and established ecosystem reinforces both network effects and high switching costs, creating strong structural protection for incumbent players.

Industry consolidation across technology generations. Historical industry dynamics point to increasing consolidation over successive DDR generations. The number of viable suppliers has declined rather than expanded: Intel exited after DDR2 due to insufficient returns, and Texas Instruments followed after DDR3. The remaining players have each invested billions of dollars over multiple DDR cycles in IP, engineering capabilities, and foundry partnerships. For potential new entrants, the combination of deep technical expertise requirements, lengthy qualification cycles, and the risk of missing critical generational transitions, which has historically proven fatal, results in prohibitively high barriers to entry.

EXHIBIT 36: **Well-established ecosystem ties and close collaboration requirements have formed high barriers that safeguard incumbents in the core memory interface chips sector**



Source: Yole, Bernstein analysis

FUTURE TECHNOLOGY ROADMAP

DDR6 AND ITS IMPLICATIONS FOR MEMORY INTERFACE CHIPS

JEDEC completed the initial DDR6 specification draft at the end of 2024, with final ratification expected within 2026. Compared with DDR5, DDR6 introduces two fundamental architectural changes. First, the peak data rate roughly doubles for the basic format: DDR6's JEDEC spec defines a base rate of 8,800 MT/s scaling up to 17,600 MT/s, versus DDR5 RDIMM's range of 4,800–8,400 MT/s. Second, DDR6 replaces DDR5's dual 32-bit sub-channel architecture with a quad 24-bit sub-channel design. By splitting data transfer across four narrower channels, each bit line is shorter and experiences less capacitance and crosstalk, enabling the data rate doubling without proportional increases in power consumption. DDR6 is also expected to adopt the CAMM2 connector standard, replacing decades-old DIMM and SO-DIMM form factors, which could change the physical design and BOM for memory modules, including the role of on-module interface chips.

All three major DRAM manufacturers — Samsung, SK hynix, and Micron — have kicked off DDR6 development, completed prototype chip designs, and are now working with memory controllers and CPU platform players on interface testing. However, commercialization timelines remain uncertain and diverge significantly across the industry: SK hynix's public roadmap, disclosed at its AI Summit in November 2025, positions DDR6 in the 2029–2031 timeframe, reflecting its strategic priority of extending DDR5 through MRDIMM and HBM4/5 for AI workloads. Next-generation CPU platforms from Intel and AMD are reportedly undergoing DDR6 interface validation, though neither has disclosed a clear product roadmap with confirmed DDR6 support. On the memory interface chip side, none of the three major vendors has yet disclosed concrete DDR6 interface chip products. Montage claims it is conducting DDR6-related R&D programs. Historically, interface chip development lags the DRAM standard by one to two years, as vendors require a stable specification before committing silicon design resources.

Critically, DDR6's base data rate of 8,800 MT/s is equivalent to the effective throughput of DDR5 MRDIMM Gen 1, while DDR5 MRDIMM Gen 3 is expected to match DDR6's high-end spec at 17,600 MT/s. It means the full DDR6 data rate range is already achievable within the DDR5 generation through advanced interface chip architectures; hence, this substantial overlap weakens the near-term urgency for server OEMs and CSPs to migrate to DDR6. This dynamic reinforces our projection that DDR5 MRDIMM penetration will continue to rise through the decade, before DDR6 becomes a compelling alternative. Looking further ahead, the outlook for DDR6 is structurally positive for the memory interface chip industry. For DDR6 to offer a meaningful bandwidth advantage over DDR5 MRDIMM, it will need to push data rates well beyond the current 17,600 MT/s ceiling of its basic specification, achieving that will require a new generation of advanced memory interface chips for active retiming, signal conditioning, and multiplexed-rank architectures analogous to what MRDIMM brought to DDR5. In other words, DDR6 in its basic module format does not offer a compelling upgrade path over DDR5 MRDIMM; only with higher interface chip content can DDR6 unlock data rates that justify the generational transition. This ensures that each successive push for higher memory bandwidth demands greater interface chip intelligence and dollar content per module, a secular trend that is positive for Montage, Renesas, and Rambus regardless of which DDR generation dominates.

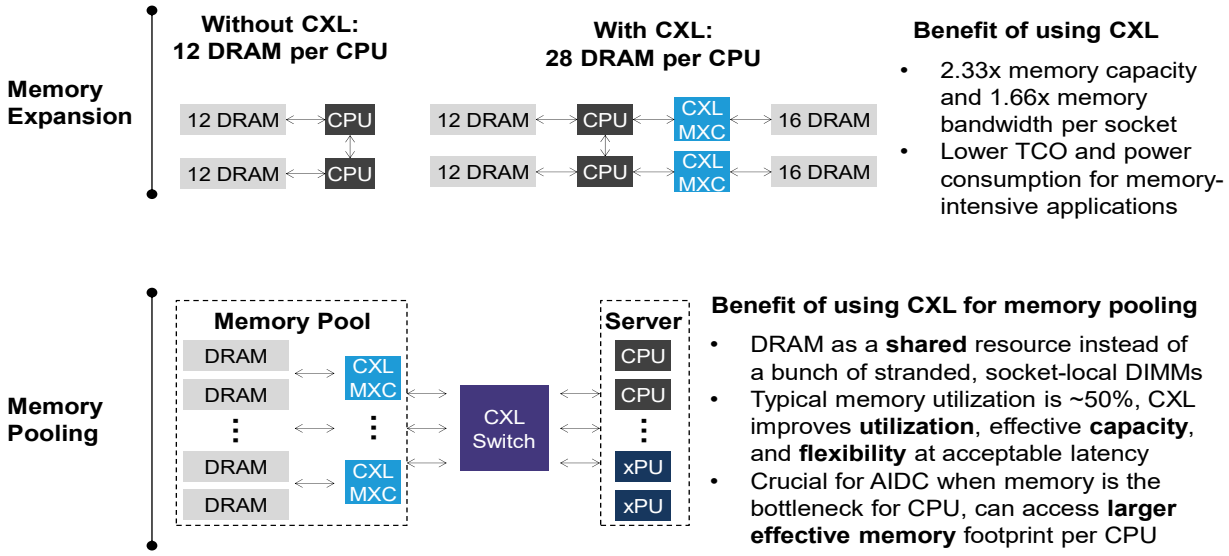
CXL: THE NEXT FRONTIER FOR MEMORY INTERFACE

As server CPU core counts have scaled aggressively over the past decade, memory bandwidth and capacity per core have not kept pace — a gap widely referred to as the "memory wall." Compounding this, a significant portion of installed DRAM in datacenter servers sits idle because the CPU cores associated with that memory are already fully allocated, a phenomenon known as memory stranding. Compute Express Link (CXL) has emerged as the industry's leading open interconnect standard to address these inefficiencies. Built on the PCIe 5.0 physical layer, CXL enables cache-coherent memory expansion and pooling, allowing disaggregated memory resources to be decoupled from host processors and dynamically shared across multiple compute nodes.

CXL serves two primary use cases: memory expansion and memory pooling. Memory expansion allows a CPU to access additional DRAM beyond its native DDR channel limits through CXL-attached memory modules, meaningfully increasing both effective capacity and bandwidth per socket. Memory pooling goes a step further by enabling shared DRAM pools, connected via CXL switches, that can be accessed by multiple CPUs or accelerators on demand. Given that typical server memory utilization hovers around 50%, pooling has the potential to substantially improve resource efficiency and lower total cost of ownership for cloud operators. Early estimates suggest first-generation CXL deployments could reduce DRAM procurement requirements by roughly 10%, with savings potentially exceeding 35% as more advanced pooling capabilities under CXL 3.0

mature.

EXHIBIT 37: **CXL has two core functions, which expand memory capacity and reduce memory stranding**



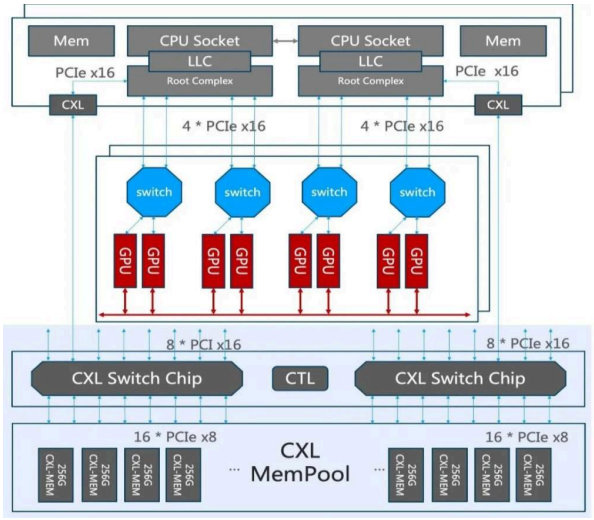
Source: company reports, Bernstein analysis

The CXL ecosystem has gained broad industry support, but mass adoption remains in early stages. The CXL Consortium now counts over 180 members spanning CPU vendors, memory manufacturers, cloud providers, and chip companies. On the platform side, both Intel and AMD have integrated CXL support into their server CPU roadmaps starting from Sapphire Rapids and Genoa, respectively. Major DRAM manufacturers including Samsung, SK Hynix, and Micron have developed CXL-compatible memory expansion modules. Certain hyperscalers have also begun piloting CXL-based architectures for next-generation server designs. The standard has evolved rapidly — from CXL 1.0 in 2019 to CXL 3.0 in 2022 — with each generation adding more sophisticated capabilities such as multi-level switching, peer-to-peer communication, and rack-scale disaggregation. CXL 3.0, built on the PCIe 6.0 physical layer, doubles transfer rates to 64 GT/s and introduces the fabric-level capabilities needed for full memory composability.

However, meaningful barriers remain before CXL can scale to broad deployment. CXL introduces an additional latency penalty of roughly 67–87 nanoseconds compared to locally attached DRAM, which confines its practical applicability to infrequently accessed memory tiers rather than latency-sensitive hot data. In AI-centric workloads, CXL also faces a fundamental bandwidth disadvantage against purpose-built accelerator interconnects such as NVLink, which delivers substantially higher bandwidth per area. This positions CXL's strongest opportunity squarely in CPU-centric general-purpose server environments rather than GPU-centric AI training clusters. Furthermore, the cost-benefit case for CXL at datacenter scale has yet to be validated in production, and product roadmap visibility for CXL 3.0-based solutions remains limited.

EXHIBIT 38: **Alibaba is one of the pioneers in adopting CXL for AIDC**

CXL-based interconnect architecture of general-purpose computing supernodes from Alibaba



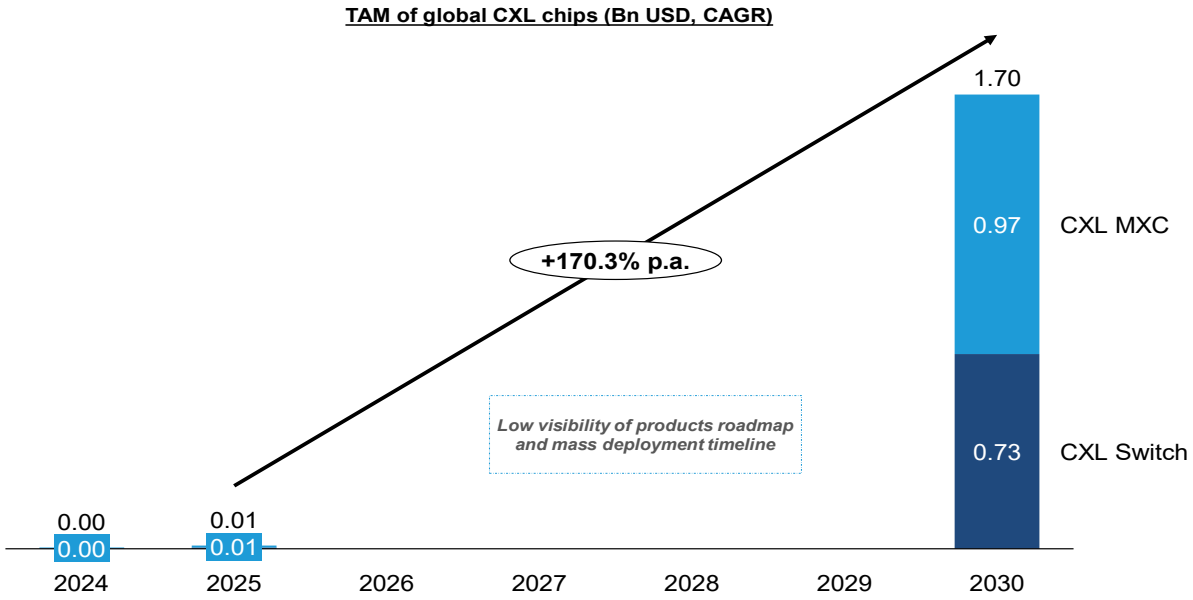
Alibaba's Panjiu CXL-based server prototype



Source: Alibaba reports, Bernstein analysis

From a competitive standpoint, CXL represents a natural adjacency for both PCIe chip vendors and memory interface chip incumbents. Since CXL shares the PCIe physical layer, companies with existing PCIe IP portfolios, including Broadcom, Astera Labs, Microchip, and Marvell, have a ready entry path into CXL silicon. Among the core memory interface chip vendors, Montage currently offers CXL memory expander controller, positioning it to extend beyond DDR-centric connectivity into the broader domain of memory networking. Rambus has gained CXL exposure through its acquisition of Xconn. The potential addressable market for CXL chips, encompassing both memory expander controllers and CXL switches, could reach up to USD 1.7 billion by 2030, though the pace of deployment remains highly uncertain. We view CXL as a potential TAM upside opportunity for the memory interface chip industry, but one whose timing and magnitude are contingent on ecosystem maturation and hyperscaler adoption decisions.

EXHIBIT 39: **The potential TAM of CXL chips can reach USD 1.7Bn by 2030, though the deployment timeline remains uncertain**



Source: Montage H share prospectus, Bernstein analysis

SOCAMM2 - NVIDIA BESPOKE DRAM FORMAT FOR ITS CPU PLATFORMS

In our latest SOCAMM2 report, we argue that **NVIDIA's adoption of SOCAMM2 in its next-generation Vera CPU represents a platform-specific architectural optimization rather than a disruptive industry-wide memory standard**. SOCAMM2 replaces the soldered LPDDR5X memory used in Grace processors with a modular LPDDR5X-based design, improving serviceability, upgrade flexibility, and multi-vendor sourcing while retaining the power-efficiency advantages of LPDDR. However, the benefits of SOCAMM2 are closely tied to NVIDIA's vertically integrated, rack-level AI system architecture, and we therefore expect its adoption to remain largely confined to NVIDIA platforms over the foreseeable future.

From a technology perspective, SOCAMM2 delivers compelling advantages in power efficiency, form factor, and bandwidth-per-watt, making it well suited for GPU-centric AI servers where system power budgets are increasingly constrained. However, **DDR5 MRDIMM continues to maintain a clear advantage in both memory bandwidth and capacity, while benefiting from a mature ecosystem and broad industry support**. Given the substantial switching costs associated with redesigning memory controllers, platform architectures, qualification processes, and software ecosystems, **we believe mainstream x86 platforms and most non-NVIDIA ARM server platforms will continue to adopt DDR5 RDIMM and MRDIMM solutions rather than migrate to SOCAMM2**.

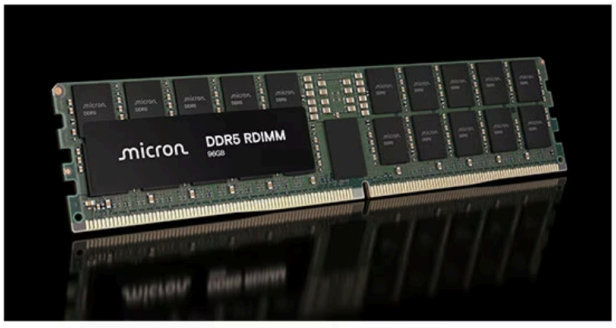
EXHIBIT 40: **Spec comparison across DDR5 RDIMM, MRDIMM, and SOCAMM2**

Superior *Moderate* *Inferior*

	DDR5 RDIMM (Gen 3)	DDR5 MRDIMM (Gen 2)	LPDDR5x SOCAMM2 for NV Vera (original design)	LPDDR5x SOCAMM2 for NV Vera (adjusted design)
Data rate	6,400 MT/s (Gen 3)	12,800 MT/s (Gen 2)	9,600 MT/s	
Aggregated bandwidth for CPU	819.2 GB/s for 16-channel CPU (6400*64 bit*16-ch/8)	1,638.4 GB/s for 16-channel CPU (12800*64bit*16-ch/8)	1,228.8 GB/s for NV Vera (9600*128bit*8 modules/8)	
Memory capacity per module	16/32/64/96/128/256 GB	128/256/512 GB	192 GB	96 GB
Total capacity per CPU	Up to 8TB+ (16-ch * 2 DIMM/Ch * 258GB)	Up to 16TB+ (16-CH * 2 DIMM/Ch * 512GB)	1.5TB (8 SOCAMM2 * 192GB)	0.75TB (8 SOCAMM2 * 96GB)
Power efficiency	Moderate ~1.1v	Higher than RDIMM – due to additional interface chips	Best-in-class – 1.05V (total energy consumption 30% lower than RDIMM)	
Compactness	288 pins, requiring vertical slot space	Similar to RDIMM	Highly compact low-profile compression module, smaller footprint	
Price per GB	$24.3	$50-75 (small sampling price)	$29 (small sampling price)	
Per module price	$3,200+ (128GB)	$6,000-9,000 (128GB)	$5,600 (196GB)	$2,800 (96GB)
Interface chip content	1 RCD + SPD + PMIC + TS (~$7)	1 MRCD + 10 MDB + SPD + PMIC + 2TS (~$50-70)	Minimal – 1 SPD + 3 voltage regulators; direct-attach without RCD/DB chips (a few dollars)	

Source: companies reports, Bernstein analysis

EXHIBIT 41: **configuration comparison between SOCAMM2 and DDR5 RDIMM**



- ~133mm x ~31mm x ~2.5mm
- 288 pins on edge connector
- Vertical, insertion socket



- ~86mm x ~14mm x ~1mm
- 694 pins on back
- Horizontal, screw mounted

Source: AMD website, Bernstein analysis

In summary, SOCAMM2 excels in power efficiency and compact design, closely aligning with NVIDIA's overarching strategy of rack-level vertical integration and maximizing tokens per second per watt. By comparison, DDR DIMMs maintain advantage in bandwidth and capacity, backed by a more established and mature ecosystem.

For memory interface chip suppliers, we view the impact of SOCAMM2 as manageable. SOCAMM2 introduces incremental chipset content versus soldered LPDDR, but value per module is only a few dollars, far below DDR5 MRDIMM's

interface silicon content at 50-70 USD. Therefore, if SOCAMM2 were to achieve broad industry adoption, the memory interface chip TAM would likely be lower. Yet if the package design will remain niche to Nvidia, then the impact to TAM will be limited to the Nvidia CPU vol share (HSD to LT%). Small incremental MRDIMM adoption could easily offset that impact. Additionally, SOCAMM2 also use some memory interface chip so the shift from LPDDR5 to SOCAMM2 within Nvidia actually brings some upside to the memory interface TAM. Rambus holds first-mover advantage at this stage, but we expect Renesas and Montage to catch up quickly given the relatively low technical barriers in SOCAMM2 interface chips.

APPENDIX - FINANCIAL FORECASTS

EXHIBIT 42: **Montage: projected income statement**

INCOME STATEMENT	FY 2021	FY 2022	FY 2023	FY 2024	FY 2025	FY 2026	FY 2027	FY 2028	FY 2029	FY 2030
Revenue	**2,562**	**3,672**	**2,286**	**3,639**	**5,456**	**7,733**	**13,552**	**25,211**	**41,966**	**58,298**
Revenue YoY%		43%	(38%)	59%	50%	42%	75%	86%	66%	39%
Revenue QoQ%										
Quarterly revenue mix										
Cost of sales (enter as -)	(1,330)	(1,967)	(939)	(1,524)	(2,061)	(2,500)	(4,564)	(8,833)	(15,429)	(22,466)
Gross Profit	**1,232**	**1,706**	**1,347**	**2,115**	**3,395**	**5,233**	**8,988**	**16,378**	**26,537**	**35,832**
Gross profit margin%	*48.1%*	*46.4%*	*58.91%*	*58.13%*	*62.2%*	*67.7%*	*66.3%*	*65.0%*	*63.2%*	*61.5%*
YoY Bp Δ		*-164 bps*	*1247 bps*	*-78 bps*	*410 bps*	*544 bps*	*-135 bps*	*-136 bps*	*-173 bps*	*-177 bps*
Other Operating Income	76	1	2	12	116	56	71	71	71	71
Selling Expenses	(45)	(86)	(90)	(96)	(118)	(139)	(163)	(184)	(203)	(220)
General & admin expenses	(198)	(208)	(179)	(203)	(480)	(400)	(452)	(497)	(542)	(585)
Total SG&A	**(243)**	**(295)**	**(269)**	**(299)**	**(598)**	**(539)**	**(614)**	**(681)**	**(745)**	**(805)**
Research and development expenses	(370)	(563)	(682)	(763)	(915)	(1,125)	(1,361)	(1,606)	(1,895)	(2,236)
Other Operating Expense	(42)	(356)	(199)	(19)	(28)	(94)	(141)	(201)	(287)	(371)
Total operating expenses	**(655)**	**(1,214)**	**(1,150)**	**(1,081)**	**(1,541)**	**(1,757)**	**(2,116)**	**(2,487)**	**(2,926)**	**(3,412)**
Expenses analysis & assumptions										
Selling Expense YoY growth		92%	4%	7%	23%	18%	17%	13%	10%	8%
Admin Expense YoY growth		5%	(14%)	13%	137%	(17%)	13%	10%	9%	8%
SG&A Ratio	(9%)	(8%)	(12%)	(8%)	(11%)	(7%)	(5%)	(3%)	(2%)	(1%)
R&D YoY growth		52%	21%	12%	20%	23%	21%	18%	18%	18%
Financial income/ (expenses) as % of b		*2%*	*3%*	*4%*	*4%*	*4%*	*3%*	*3%*	*3%*	*3%*
Investment income as % of beginning b		(1%)	(0%)	(1%)	(1%)	(4%)	(4%)	(4%)	(4%)	(4%)
Other gain / (loss) as of sales	*1%*	*(10%)*	*(9%)*	*(0%)*	*2%*	*(0%)*	*(1%)*	*(1%)*	*(1%)*	*(1%)*
Total Operating Expenses Ratio	*(26%)*	*(33%)*	*(50%)*	*(30%)*	*(28%)*	*(23%)*	*(16%)*	*(10%)*	*(7%)*	*(6%)*
Operating profit	**653**	**493**	**199**	**1,046**	**1,971**	**3,531**	**6,943**	**13,962**	**23,681**	**32,491**
Operating profit margin	*25.5%*	*13.4%*	*8.7%*	*28.8%*	*36.1%*	*45.7%*	*51.2%*	*55.4%*	*56.4%*	*55.7%*
Interest Income (Expense)	72	81	179	230	269	377	485	576	752	1,022
Income (Loss) from Affiliates	(6)	(4)	(4)	(7)	(15)	(41)	(55)	(55)	(55)	(55)
Non-operating activities	196	843	98	143	95	150	--	--	--	--
Pretax profit	**915**	**1,414**	**472**	**1,413**	**2,321**	**4,017**	**7,373**	**14,482**	**24,378**	**33,458**
Taxes (enter expense as -)	(86)	(114)	(21)	(72)	(191)	(393)	(885)	(1,883)	(3,413)	(5,019)
Effective tax rate	*(9.4%)*	*(8.1%)*	*(4.5%)*	*(5.1%)*	*(8.2%)*	*(9.8%)*	*(12.0%)*	*(13.0%)*	*(14.0%)*	*(15.0%)*
Net Profit (incl. minority interest)	**829**	**1,299**	**451**	**1,341**	**2,130**	**3,624**	**6,488**	**12,600**	**20,965**	**28,439**
Loss/(gain) attributable to the noncontrolli	--	(0)	0	(71)	(106)	(97)	(106)	(106)	(106)	(106)
Minority interest as % of net profit	-	(0.0%)	0.1%	(5.3%)	(5.0%)	(2.7%)	(1.6%)	(0.8%)	(0.5%)	(0.4%)
Profit attributable to equity owners of	**829**	**1,299**	**451**	**1,412**	**2,236**	**3,721**	**6,594**	**12,706**	**21,071**	**28,545**
Net profit margin%	*32.4%*	*35.4%*	*19.7%*	*38.8%*	*41.0%*	*48.1%*	*48.7%*	*50.4%*	*50.2%*	*49.0%*
Net Profit YoY		*57%*	*(65%)*	*213%*	*58%*	*66%*	*77%*	*93%*	*66%*	*35%*
Extraordinary gain/ (loss)	--	--	--	--	--	--	--	--	--	--
Basic EPS	0.73	1.15	0.40	1.25	1.97	3.21	5.68	10.82	17.93	24.04
Diluted EPS	0.73	1.15	0.40	1.25	1.96	3.15	5.55	10.70	17.73	24.01
Basic EPS YoY		**58%**	**(65%)**	**213%**	**58%**	**63%**	**77%**	**91%**	**66%**	**34%**
Dividends	339	339	341	338	670	1,674	2,967	5,718	10,536	14,273
DPS	0.30	0.30	0.30	0.39	0.59	1.42	2.50	4.81	8.86	12.02

Source: Bloomberg, Bernstein analysis and estimates

EXHIBIT 43: **Montage: projected balance sheet**

BALANCE SHEET	2021	2022	2023	2024	2025	2026E	2027E	2028E	2029E	2030E
Assets										
Cash & equivalents	5,087	5,834	5,666	6,699	8,471	16,554	19,083	24,502	32,703	44,595
Financial assets held for trading	414	1,610	1,703	1,783	823	2,131	2,131	2,131	2,131	2,131
Accounts & other receivables, prepaym	172	322	294	388	568	753	1,319	2,453	4,083	5,672
Inventories	375	738	482	352	896	888	2,410	4,660	8,137	11,846
Other current assets	1,375	132	150	239	276	532	638	753	889	1,042
Total current assets	**7,423**	**8,636**	**8,296**	**9,461**	**11,034**	**20,858**	**25,582**	**34,500**	**47,944**	**65,286**
Total PP&E, intangible assets, ROU an	1,178	779	1,094	1,445	1,454	1,308	1,146	1,057	1,016	1,009
Long-term equity investment	290	1,149	1,207	1,226	1,080	1,376	1,376	1,376	1,376	1,376
Goodwill	--	--	--	--	--	--	--	--	--	--
Other non-current assets	68	122	101	86	180	194	194	194	194	194
Total non-current assets	**1,536**	**2,050**	**2,401**	**2,758**	**2,714**	**2,878**	**2,716**	**2,627**	**2,587**	**2,580**
Total assets	**8,959**	**10,686**	**10,698**	**12,219**	**13,748**	**23,736**	**28,298**	**37,127**	**50,531**	**67,866**
Liabilities and Shareholder's Equity										
Accounts payables and other payables	424	605	376	642	755	1,156	2,019	3,904	6,816	9,923
Short-term borrowings	13	12	13	16	15	17	17	17	17	17
Contract Liabilities	--	--	--	--	1	2	2	2	2	2
Other current liabilities	--	23	2	22	0	0	0	0	1	1
Total Current Liabilities	**437**	**639**	**391**	**680**	**770**	**1,175**	**2,038**	**3,923**	**6,835**	**9,943**
Long-term borrowings	20	9	2	29	19	66	66	66	66	66
Other non-current liabilities	111	111	98	114	88	85	85	85	85	85
Total Non Current Liabilities	**131**	**119**	**100**	**143**	**107**	**152**	**152**	**152**	**152**	**152**
Total liabilities	**568**	**759**	**491**	**822**	**877**	**1,326**	**2,189**	**4,074**	**6,987**	**10,094**
Capital Reserve & Additional Add-in Ca	5,866	1,134	1,139	1,145	6,118	1,222	1,222	961	961	699
Less: Treasury Stock	(300)	(300)	(300)	(428)	(848)	(848)	(848)	(587)	(587)	(325)
Retained earnings / (accumulated defic	2,646	3,622	3,732	4,805	6,371	8,798	12,425	19,413	29,949	44,222
Other comprehensive income / (loss)						--	--	--	--	--
Other equity tools	179	5,456	5,621	5,881	1,283	13,387	13,565	13,627	13,688	13,750
Total Shareholders Equity	**8,391**	**9,912**	**10,191**	**11,403**	**12,924**	22,560	26,364	33,414	44,011	58,345
Minority shareholders' interest	--	15	15	(7)	(53)	(150)	(256)	(362)	(467)	(573)
Total Equity	**8,391**	**9,927**	**10,207**	**11,397**	**12,871**	**22,410**	**26,109**	**33,053**	**43,544**	**57,772**
Total Liabilities & Equity	**8,959**	**10,686**	**10,698**	**12,219**	**13,748**	**23,736**	**28,298**	**37,127**	**50,531**	**67,866**

Source: Bloomberg, Bernstein analysis and estimates

CASH FLOW STATEMENT	2021	2022	2023	2024	2025	2026E	2027E	2028E	2029E	2030E
Net Income	829	1,299	451	1,341	2,130	3,721	6,594	12,706	21,071	28,545
Depreciation and Amortization	59	52	105	141	120	469	504	451	424	414
SBC & Others	243	(271)	193	(23)	361	133	178	62	62	62
Change in net working capital	(155)	(392)	(18)	162	(668)	**(119)**	**(1,332)**	**(1,614)**	**(2,330)**	**(2,344)**
Cash from operating activities	**975**	**689**	**731**	**1,691**	**2,048**	**4,204**	**5,944**	**11,604**	**19,227**	**26,677**
Net capex	(153)	(226)	(424)	(379)	(266)	(322)	(342)	(362)	(384)	(407)
Cash paid for equity investment	—	—	--	—	—	--	--	--	--	--
Other investments	(72)	290	(150)	(64)	1,090	(1,379)	--	--	--	--
Cash from investing activities	**(226)**	**63**	**(574)**	**(443)**	**824**	**(1,701)**	**(342)**	**(362)**	**(384)**	**(407)**
Change in debt	--	(13)	(16)	(21)	--	51	--	--	--	--
Change in equity	(270)	82	(15)	83	(359)	7,094	--	(262)	--	(262)
Cash Paid for Distribution of Dividends, P	(339)	(339)	(341)	(338)	(670)	(1,674)	(2,967)	(5,718)	(10,536)	(14,273)
Other Cash Paid Related to Financing Ac	--	--	--	--	--	(79)	(106)	156	(106)	156
Cash from financing activities	**(609)**	**(270)**	**(372)**	**(277)**	**(1,029)**	5,773	(3,073)	(5,823)	(10,642)	(14,379)
Exchange Gains (losses) on Net Cash	(61)	268	47	62	(126)	(141)	--	--	--	--
Net change in cash during period	**79**	**750**	**(168)**	**1,033**	**1,717**	**8,135**	**2,529**	**5,419**	**8,202**	**11,891**

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VALUATION METHODOLOGY

Montage Technology

We set our **A-share TP at CNY 400**, based on **50x 2BF P/E** (27Q3–28Q2 earnings). We raise our 2027/2028 EPS estimates to CNY 5.68/10.82, respectively, on a stronger outlook for the CPU cycle and MRDIMM penetration. For the **H shares**, we set a target price of **HKD 520**, implying a **15% premium** to our A-share TP (we use the CNY to HKD exchange rate at 1:1.13). The H share premium reflects that global investors favor Montage as a scarce China AI-exposed name without direct geopolitical risks, unlike many other Chinese semiconductor companies that face entity list restrictions or export control headwinds. At our target price, the implied P/E multiple on 2BF EPS for H shares is 58x.

Renesas Electronics Corp

We set a ¥6,300 target price using a P/E multiple of 20x against our forward Q5-Q8 EPS estimate of ¥316.

RISKS

Montage Technology

Key potential risks:

1. A decrease in memory and AIDC server demand;
2. Intensify competition that leads to share loss and lower margin;
3. Failure to introduce new products for the AIDC networking market.

Renesas Electronics Corp

There are a number of downside risks to our Renesas target price: (1) Prolonged delay in the Analog market recovery (2) Weaker-than-expected market share gain in both Automotive MCU and AI power markets (3) Exchange rate fluctuation with upside / downside risk to overall Japan market.

RATINGS DEFINITIONS, BENCHMARKS AND DISTRIBUTION

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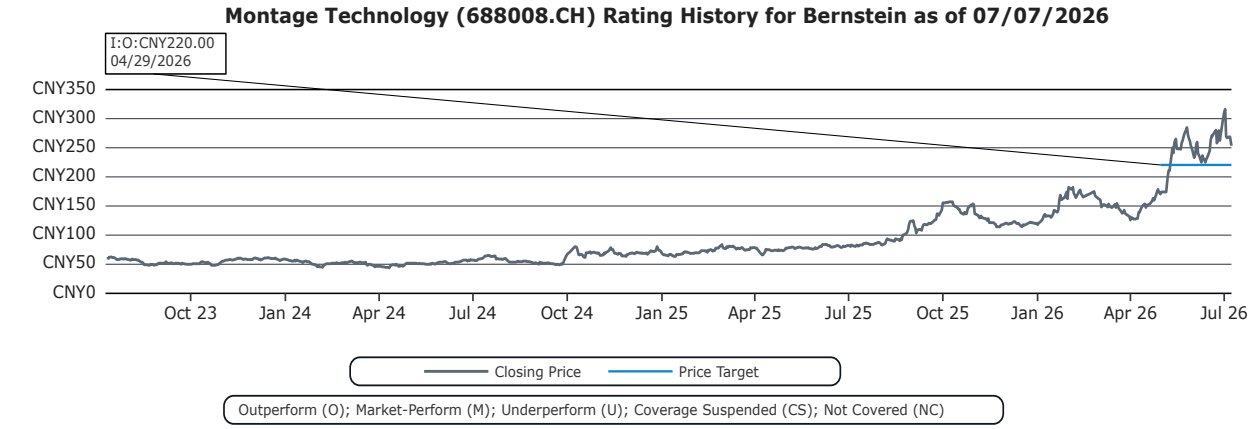
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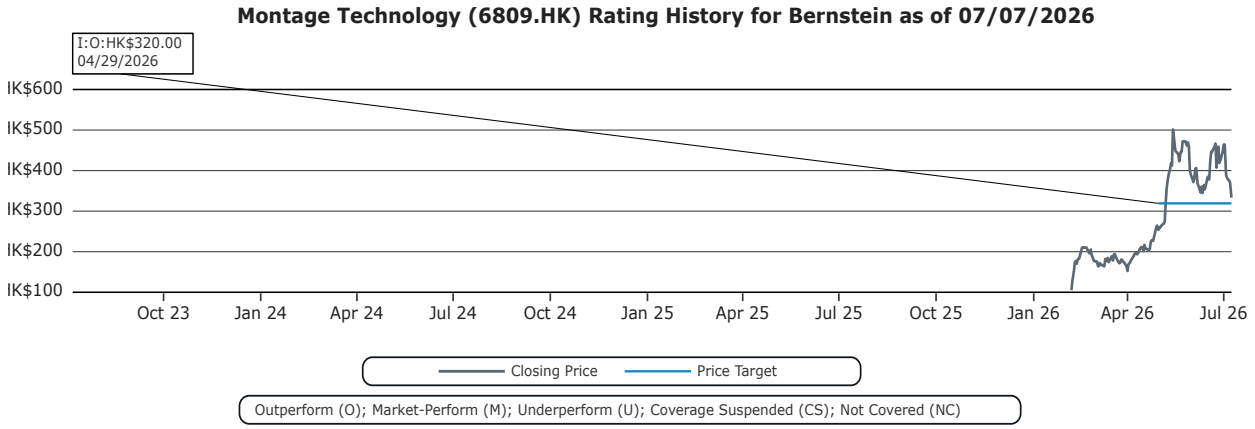
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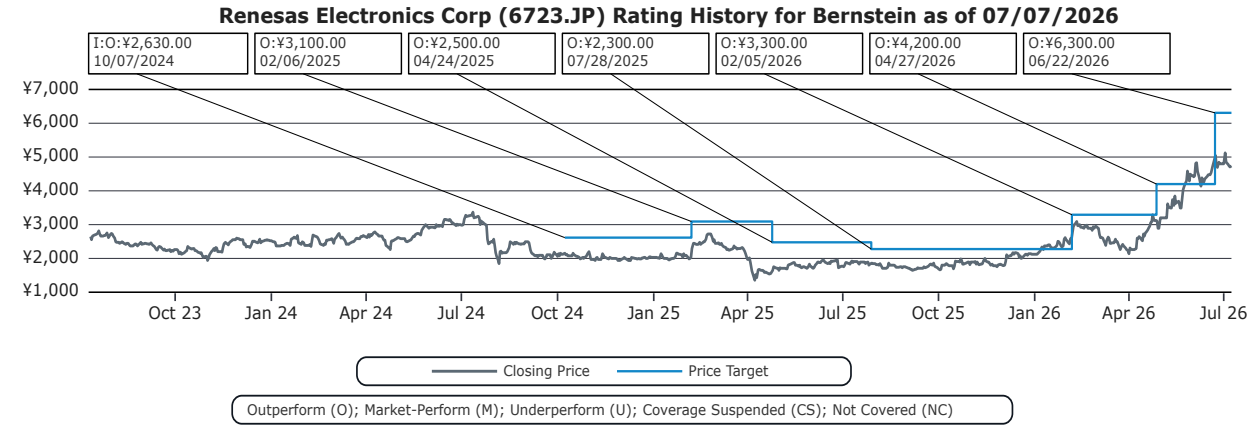
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