BERNSTEIN
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China Semiconductors

China Semis: Huawei's Tau (τ) Law, another DeepSeek moment



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Huawei unveiled the **"Tau (τ) Scaling Law"** at ISCAS 2026 on May 25, 2025, proposing a shift from geometric scaling (making transistors smaller) to temporal scaling (reducing signal latency) as a successor to Moore's Law. A-share semis names rallied yesterday (STAR 50 +5.9%). We believe the Tau law demonstrates that China is making impressive tech breakthrough despite export controls, and sets a clear roadmap for continuous improvement in chip performance without EUV, making it another DeepSeek moment for China Semis. **Reiterate Outperform for the sector.**

Tau Law demonstrates breakthrough beyond what's achieved. The core idea of the Tau law is systematically reducing the time constant τ by cutting signal latency across entire semis stacks. One of Huawei's tech innovation called '**LogicFolding**' looks similar to TSMC's SoIC at first glance, as they both stack two dies on top of each other. But Huawei is able to achieve impressive sub-2um bonding pitch (Exhibit 2), which allow them to stack logic on top of logic to reduce latency (cell to cell) rather than just stack up at chip level (die to die, usually SRAM on logic). This is why they are able to improve not only on density but also on frequency (Exhibit 1). On top of that, Huawei emphasizes the importance of end-to-end co-optimization for AI, where the improvement across the transistor-circuit-chip-system levels are all leveraged. They target to achieve 125X compute power improvement at superPoD level in the next five years through **near-packaged optical** I/O ('Hi-ONE') and **Unified Bus** networking (Exhibit 3). With these improvements across different tech stacks, they are able to deliver massive performance improvement at the cluster level, which is what the customers actually needs. Therefore, we think of Tau law as a predictable and scalable roadmap metric to guide the China Semis to go beyond the EUV constrain and continuously improve for the next decade.

However, Tau Law comes with constraints and won't allow China to close the gap with global leaders yet. First, Tau Law assumes sustained progress in 3DIC advanced packaging, areas where global leaders like TSMC still hold a meaningful technology and ecosystem lead. Second, stacking multiple dies boosts transistor density but also increases power density, thermal constraints will be a key issue that require power-delivery innovations. Thirdly, the yield and cost will also be another barrier for adoption if not engineered properly. Arguably the innovations from Huawei are the ones that global players can copy, but Huawei won't have EUV anytime soon yet, so China will be still behind global leaders in semis, although we do see that these innovations could allow Huawei to continuously improve and gradually narrow the gap. The differentiation for Huawei will likely come down to how fast they can solve these challenges, integrate the stacks more tightly, and scale manufacturing reliably and economically.

The upside for China semis is massive if the Tau Law is executed successfully. Just like DeepSeek innovation on algorithm encouraged China to invest in AI and build a whole AI-stack locally, Huawei's Tau Law now will give the industry a lot more confidence to invest in China semis and build a whole Semis-stack locally, further enhancing our localization thesis for the sector. We like **SMIC, NAURA, Piotech** the most under this theme, as SMIC executes the advanced logic and packaging manufacturing, NAURA delivers the tools for advanced logic fabrication, and Piotech could potentially support the bonding tools for the LogicFolding design.

BERNSTEIN TICKER TABLE

Ticker	Rating	Cur	25 May 2026 Closing Price	Price Target	TTM Rel. Perf.	Reported EPS Cur	2025A	2026E	2027E	Reported P/E (x) 2025A	2026E	2027E
688981.CH (SMIC-A)	O	CNY	156.00	120.00	45.0%	USD	0.09	0.10	0.13	267.6	229.1	182.0
981.HK (SMIC-H)	O	HKD	79.85	70.00	48.8%	USD	0.09	0.10	0.13	118.8	101.7	80.8
688347.CH (Hua Hong-A)	O	CNY	214.80	140.00	305.3%	USD	0.03	0.11	0.16	995.5	297.0	203.4
1347.HK (Hua Hong-H)	O	HKD	130.10	100.00	271.1%	USD	0.03	0.11	0.16	523.1	156.0	106.9
002371.CH (NAURA)	O	CNY	698.19	680.00	77.8%	CNY	5.66	10.22	16.41	123.3	68.3	42.6
688012.CH (AMEC)	O	CNY	485.30	500.00	137.5%	CNY	3.40	4.95	7.18	142.7	98.1	67.6
688072.CH (Piotech)	O	CNY	721.00	580.00	341.6%	CNY	3.32	8.12	12.40	217.2	88.8	58.2
688256.CH (Cambricon)	O	CNY	1,406.50	2,000.00	181.3%	CNY	(1.09)	5.38	11.26	N/M	261.2	124.9
688041.CH (Hygon)	O	CNY	329.68	280.00	101.5%	CNY	0.83	1.35	2.42	397.2	244.3	136.3
ASIAX			1,939.99									

O - Outperform, M - Market-Perform, U - Underperform, NR - Not Rated, CS - Coverage Suspended

688256.CH, 688041.CH base year is 2024;

Source: Bloomberg, Bernstein estimates and analysis.

INVESTMENT IMPLICATIONS

We rate SMIC, Hua Hong, NAURA, AMEC, Piotech, Cambricon, Hygon Outperform benefiting from this new roadmap for China Semis.

On beneficiaries, we see the Tau Law roadmap as structurally positive for China's leading foundry, advanced-packaging supply chain, and AI chip ecosystem. On foundry, **SMIC** is a clear strategic partner and likely a critical enabler if Huawei is to deliver the roadmap and eventually reach TSMC A14-equivalent logic density via multi-die integration without EUV, implying sustained demand for SMIC's most advanced DUV based multi-patterning advanced logic nodes. **Hua Hong** likely will also benefit as the expected acquisition of Huali who is potentially also working on advanced logic packaging. In semicap, we see upside skewed to domestic tool vendors who has higher exposure for advanced logic and packaging: **NAURA** should benefit more than **AMEC** as it has much higher exposure in advanced logic, while **Piotech** has been working on bonding tools for advanced packaging and thus market will perceive it as one of the core beneficiaries. For AI fabless, Huawei's framework provides a clearer path to sustain performance scaling under EUV constraints, which should be supportive for domestic accelerator and CPU vendors such as **Cambricon** and **Hygon** as they co-optimize architectures to exploit higher effective density and lower latency interconnect within China's manufacturing envelope. On the other hand they also face more intense competition from Huawei so the upside will be smaller for the AI fabless names compared to foundry and semicap.

DETAILS

HUAWEI'S ROADMAP ON CIRCUITS AND SYSTEMS

In the event, Huawei released its roadmap for chip improvement under the guidance of Tau Scaling Law.

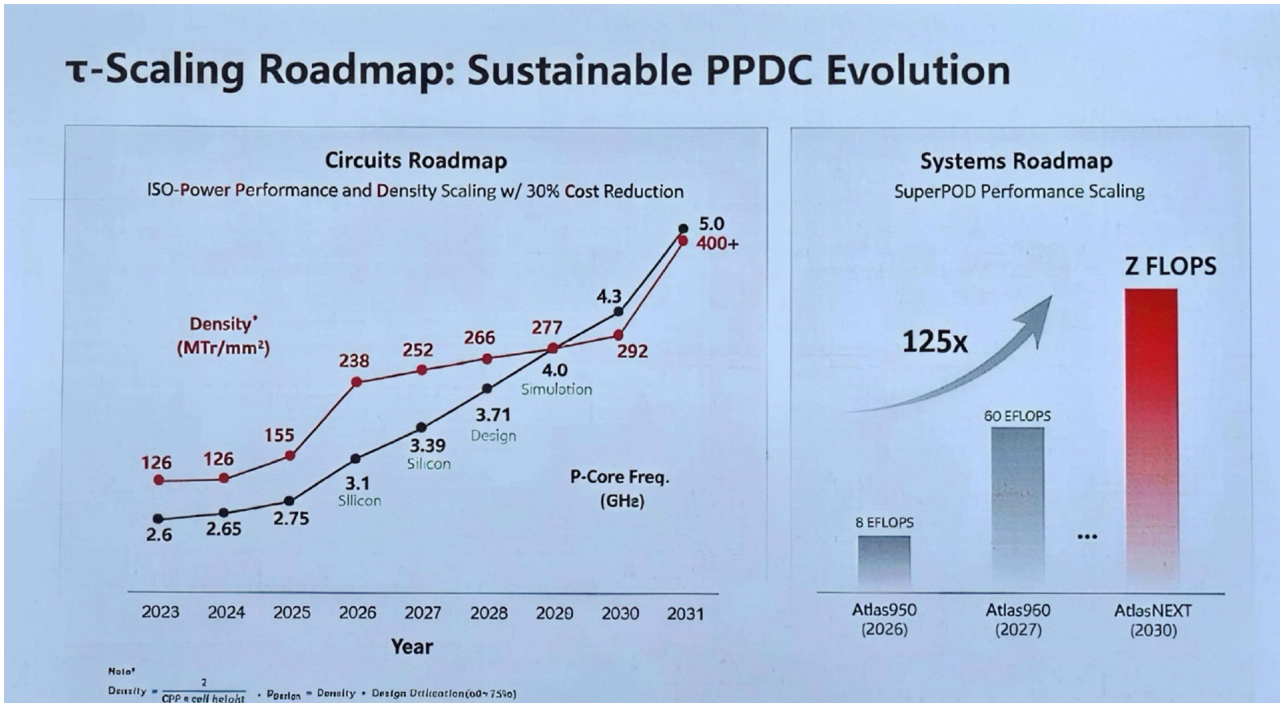
Three key highlights:

1. **Fast transistor density improvement.** Trough advanced packaging (or so-called 'LogicFolding' by Huawei), they are able to improve the transistor density from 155 MTr/mm^2 in 2025 (HiSilicon Kirin 9030, based on SMIC N+3 node, between TSMC N5 and N7) to 238 MTr/mm^2 in 2026 (equivalent to TSMC N3 node density. Likely that's based on two chips stack on top of each other, for example one SMIC N+3 node chip with another SMIC N+2 node chip, so no longer apple to apple comparison). By 2031, they target to achieve 400+ MTr/mm^2 (equivalent to TSMC 14A density, but again not apple to apple comparison);

2. **Steadily increasing max frequency.** The speed of a transistor is generally measured by how fast it can switch, or the frequency, further improvement on the max frequency is achieved through the tau optimization that reduced the latency, which is the critical-path delay between adjacent transistors, which in turn is dominated by interconnect RC;

3. **Exponentially growing AI cluster scaling.** On top of improvement on chip performance, the Tau Scaling Law also emphasizes on the improvement of networking between chips to build exponentially larger AI superPoDs, we have illustrated that in the Huawei AI chip roadmap analysis, and now Huawei targets to achieve 125X improvement in superPoD total compute power by 2030, which indicates an aggressive 3.3X improvement every year.

EXHIBIT 1: **Huawei's tau scaling roadmap**



Source: Company reports, Bernstein analysis

THE TIME SCALING THEORY

Link to the full technical paper: A Time Scaling Theory for Multi-Layer Electronic Systems

Copying the abstract here:

For six decades, Moore's geometric scaling drove progress in semiconductors. That industry compact no longer holds: returns from pure dimensional shrinking have flattened, leading-edge design budgets exceed one billion dollars per chip, and cost-per-transistor at the most advanced nodes is no longer falling. This perspective argues for a successor scaling principle — τ scaling — that adopts time itself, rather than transistor area, as the primary metric of progress, applying a single characteristic time constant τ as the unifying optimization target across twelve orders of magnitude, from a switching transistor to a data-center workload. Two production-scale demonstrations are presented. On a mobile SoC, LogicFolding — a methodology that partitions digital, analog, and memory circuits across vertically stacked active tiers — delivers a 55% step-wise increase in transistor density and a 41% power-efficiency gain at a fixed device node. On AI systems, a co-designed stack comprising the memory-semantic Unified Bus fabric, near-packaged Hi-ONE optical I/O, and edge-to-surface 3D Folding projects more than 100× growth in hardware integration by 2035. The deeper claim is methodological: τ scaling is the first scaling principle since Dennard to establish a shared optimization target across the entire computing stack.

The theory dictates optimizing and compressing delay (τ) across four collaborative layers of the compute stack:

- **Transistor Level:** Reducing intrinsic transistor switching and interconnect delays. This part is where the Moore's law has been making the direct impact, where shrinking the feature size of a transistor help to improve the speed of calculation. Beyond shrinking the size of the feature, changing the structure could also improve transistor performance (e.g. from planner to FinFET to GAA structure). We believe local foundry are also making progress at this level, such as **using DUV to manufacture GAA** structure;

- **Circuit Level:** Implementing **LogicFolding** (breaking down and vertically stacking logic, memory, and analog blocks using 3D heterogeneous integration and fine-pitch hybrid bonding) to drastically shorten critical wiring and reduce RC loads. Beyond the traditional 3DIC roadmap, Huawei further bring the design from **'Chip to Chip' stacking to 'Cell to Cell' stacking**, allow different part of the circuit function (the Combinational logic and Sequential logic, which performs the calculation and memory parts within a transistor) to be stacked on to of each other.

- **Chip Level:** Optimizing silicon and software holistically to reduce total execution time. This is commonly cited as '**Design-Technology Co-Optimization**' by the industry. As Huawei is forced to build its own know-how on process, and even build its own fabs, it's also possible that Huawei can move faster in the co-optimization to deliver better results at the chip level.

- **System Level:** Utilizing memory-semantic unified bus structures (e.g., UnifiedBus) and high-speed optical I/O (e.g., Hi-ONE) to bypass physical distance bottlenecks and compress cluster communication latency from tens of microseconds to ~100 nanoseconds. This is the networking architecture optimization illustrated in Huawei's paper on UB-Mesh (UB-Mesh: a Hierarchically Localized nD-FullMesh Datacenter Network Architecture)

Specifically, in the paper Huawei illustrates the advanced packaging technology that they rely on to get to the impressive 238 MTr/mm^2 transistor density in 2026 that likely will be deployed on its next generation mobile phone Huawei Mate90, and the networking innovations that allow Huawei to deliver more scaling capabilities for AI clusters for the next decade.

EXHIBIT 2: **Technology used for LogicFold**

Sidebar A — *LogicFolding* at a Glance

- Hybrid-bonding pitch: sub-2 μm (1.5 μm in Kirin 2026; target gear ratio ≈ 1)
- Overlay accuracy: under 0.5 μm
- TSV CD/KOZ: sub-1.5 μm; pitch sub-6 μm; failure rate <100 ppm; repair rate 99.9%
- Yield: ~100% with smart redundancy
- Transistor density: 155 →238 MTr/mm² in a single step
- Power-efficiency / frequency gain (SoC P-core): +41% / +13%
- SRAM operating frequency: +40%+
- Clock-buffer count / clock skew / wire length on a representative core: −50% / −25% /−30%

Source: Company reports, Bernstein Analysis

EXHIBIT 3: **Key technology Huawei used to improve system level tao**

Sidebar B — τ at AI System Scale

- UB remote-access latency: ~10s of μs → ~100 ns (≈ 500× τ reduction)
- HiONE per-module bandwidth: 8 Tb/s (matches per-chip UB bandwidth)
- HiONE SerDes reach: ~100 cm → ~5 cm; panel-to-panel reach: <1 m → 100 m
- Fan-out dilemma: compute $\propto N^2$, perimeter-bound BW/I/O/power $\propto N$
- 3D Folding: relocates BW, optical I/O, and power delivery from edges onto surfaces, restoring N^2 parity
- 2026 → 2035 projected hardware-integration growth: >100×

Source: Company reports, Bernstein Analysis

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