TSMC

CoWoS and Advanced Backend Updates

Overweight

2330.TW, 2330 TT
Price (15 May 26):NT$2265.0
Price Target (Dec-26):NT$2500.0

- **Raising CoWoS estimates for 2027/28; continue to expect a strong SoIC ramp:** We raise our CoWoS estimates and now expect TSMC to build 115K/175K/220K wfpm CoWoS capacity by end 2026/27/28, with upside coming from a faster ramp of in-house capacity in 2027-28 and leveraging OSATs and VIS for interposer manufacturing. We now expect TSMC's CoWoS capacity to reach 1.1/1.9mm and 2.4mn annual CoWoS wafer output in 2026/27 and 2028, respectively. With a more conservative view on CoPoS technology adoption and extension of CoWoS to larger reticle size packages (up to 14x by 2028), we now anticipate a faster CoWoS capacity ramp into 2028, aligned with TSMC's recent guidance of 80+% CAGR in CoWoS capacity over 2022-27. We continue to expect a strong ramp in SoIC reaching 40/65k wfpm by end 2027/28, as 3DSoIC packaging adoption picks up meaningfully from 2H27 for several ASICs, NVDA and CPO projects.
- **NVDA estimates up slightly due to stronger Blackwell, Spectrum X and Vera CPUs:** We nudge up our NVDA CoWoS estimates slightly for 2026 led by stronger Blackwell GB300 orders due to rising compute demand, especially from OpenAI, and a stronger-than-expected ramp for Spectrum X and Vera CPUs in 2H26. We trim Rubin numbers slightly due to uncertainties regarding HBM4 supply, but still expect product ramp in 3Q26, with meaningful volumes in 4Q26. Looking into 2027, we expect stronger growth in Rubin, continued ramp into 2-die per interposer Rubin Ultra solution, stronger growth in Vera CPUs (especially given a stronger push for standalone Vera CPU racks) and continued ramp of Spectrum X networking solutions. We believe that TSMC is likely to focus its CoWoS-L resources on Rubin and Rubin Ultra GPUs, along with Spectrum X (CPC and CPO), while Vera CPU is likely to be outsourced to OSATs in 2027 (starting with Amkor and also involving ASE). LPU is also likely to migrate to CoWoS-R in 2028, which should put additional strain on TSMC CoWoS capacity. For the Feynman GPU in 2028, initial packaging design plans from NVDA appear more conservative, with the base model likely to stick with a 2-GPU die per interposer design (similar to Rubin Ultra), while the enhanced model is likely to embrace 3D SoIC (likely stacking SRAM along with the GPU die). We now believe that Feynman is likely to stick with variants of CoWoS, rather than migrate to CoPoS.
- **Raising AMD estimates meaningfully for 2027 to reflect MI450 and Venice ramp:** AMD appears to have largely resolved its chip-level design issues for MI450 and should ramp volumes in late 2026, even considering some rack-level teething problems. We are raising our 2027 CoWoS estimates for AMD significantly to 180K wafer per year, reflecting a strong ramp for MI450 series and ongoing strong CPU demand driving Venice CPU shipments (CoWoS-L mostly migrating to ASE by 2027). ASE also appears to have several 2.5D packaging solutions for AMD (under the EFB – Elevated Fan-Out Bridge – architecture) for the PC and gaming market, which is not captured in our CoWoS forecast. Looking ahead, AMD is likely to push the boundaries of

Technology and Telecoms

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See page 10 for analyst certification and important disclosures, including non-US analyst disclosures.

CoWoS packaging with its MI500 series (in 2027-28), with the CoW package size likely approaching 14x reticle size.

- **Continued uptick in Broadcom and Mediatek estimates, reflecting TPU ramp:** We continue to see healthy momentum for Google TPUs at both Broadcom and Mediatek, and now expect total TPU shipments to reach 4.5/8M units in 2026/27. As a result, we raise our Broadcom CoWoS numbers to 250/425k wafers in 2026/27 and Mediatek estimates to 30/125k wafers. For Mediatek, the allocation continues to increase in 2027, given stronger intent from Google to ramp up the Zebrafish SKU in higher volume, per our channel checks. For TPU v9, Mediatek's Plan A is to use EMIB, but a plan-B using CoWoS-L is also gathering more momentum, while Broadcom appears to be committed to using CoWoS-L with 3D SoIC. We believe that a final decision is likely by the end of 2026. For Broadcom, we aren't seeing a strong ramp in CoWoS forecasts from other customers (Meta, OpenAI etc.) so far in 2026 or 2027.
- **AWS Trn3 remains strong, with meaningful upside in 2027, mostly through AWS/ Alchip:** We leave our Trainium estimates for 2026 largely unchanged, given lack of additional capacity availability, but demand continues to remain quite strong. As a result, we now believe that lifetime Trn3 shipments could reach 4.6-5M units, depending on incremental CoWoS-R capacity allocation. We expect at least 3M units of Trn3 shipments in 2027, with room for further upside if AWS is able to qualify OSAT vendors such as ASE for CoWoS-R full-process packaging in 2027. For now, we are seeing most of the volumes being directed through AWS direct or Alchip and do not see big CoWoS or OSAT packaging orders from other vendors, even though N3 wafer sourcing is now being allocated to several small vendors that may have secured TSMC wafer allocation.
- **CoPoS progress appears slower than previously expected:** Compared to 1-2 months ago, TSMC's progress and intent with CoPoS appears slower, in our view. The process is still in engineering qualification, and we should have firm timelines decided by end-2026. However, supply chain partners have become less confident about a ramp in CoPoS capacity to meet NVDA demand in 2H28. The lack of any mention of CoPoS in TSMC's 2026 Technology Symposium also leads us to believe in a later ramp for CoPoS than current market consensus. Current plans for AP7 Fab ramp up indicate that CoPoS will ramp up in the 2029-30 timeframe, with the near-term focus largely on SoIC (for AP7 Phases 2 and 3). Progress in panel-level packaging among other vendors also appears to be slower, including ASE and PTI (which has only secured one AMD Gaming APU project, according to our checks, likely for the next Xbox Semi-Custom chip).
- **Large Reticle Size CoWoS in 2D and rising interest in 3D SoIC are the way to go:** Surprisingly, at its Tech symposium, TSMC announced that CoWoS could go to 14x reticle size by 2028 (higher than the 8-9x maximum package size prior), with plans to advance beyond the 14x reticle limit in the future. It appears that TSMC is more comfortable extending the life of CoWoS, given some of the uncertainties that have popped up with CoPoS. At 14x reticle size, we believe that cost may become a limiting factor for certain customers, given that the process may only yield 3 packages per wafer with a significant amount of interposer area being wasted. However, we are already seeing certain customers embracing this idea (AMD MI500 likely the first one). At the same time, TSMC is also encouraging customers to migrate to chiplets and 3D SoIC packaging in the 2nm era. Moving to 3D will solve some of the packaging challenges from ever-expanding package size. We expect several ASIC vendors (TPUv9, Trainium 4, MTIA 400, Titan 2) to start using SoIC in the late 2027-28 timeframe, while some versions of NVDA Feynman will also likely adopt 3D SoIC. As a result, we see very strong growth in 3D SoIC capacity into 2028, with two new phases of capacity coming up in AP7.
- **How much of a threat is Intel EMIB to TSMC's advanced packaging dominance?** Intel's EMIB (especially EMIB-T) technology is starting to see some traction among ASIC vendors as an alternative packaging technology, in our view, given

the severe shortage of TSMC packaging capacity and the promise of lower costs with EMIB. On paper, EMIB has some advantages over CoWoS, in that: (1) it doesn't use a circular interposer and hence can be a cheaper technology, and (2) using square substrate panels enables it to scale more efficiently compared to CoWoS, which may yield much fewer packaged chips at high reticle sizes. So far, EMIB has largely been used by Intel for server CPUs, which typically have only 3-6 silicon bridges embedded into the substrate, with the very high-end versions having 10-12 silicon bridges. However, for AI accelerators, there is a need to migrate to the EMIB-T version (with embedded TSVs to support vertical signal delivery to HBM) and also add discrete silicon capacitors below the substrate layers (unlike integrated Deep Trench capacitors in CoWoS). For the marquee EMIB-based accelerator project in late 2027, TPU v9 Humufish by Mediatek, we expect the number of silicon bridges to expand to more than 25, which is likely to become a significant strain on substrate yield. Compared to TSMC CoWoS yield rates of 98+%, we believe that EMIB yields for current products are still at 90+% levels, with indicative yields for very high bridge count packages (such as for Humufish) well below these levels, which is the key variable for successful mass production ramp.

- **CPUs, LPU and networking are new drivers for CoWoS demand:** In 2026, we are seeing several new drivers for CoWoS demand emerging. NVDA Vera and AMD Venice server CPUs will start utilizing CoWoS packaging for the first time, with volumes ramping at TSMC first, in our view, and then migrating to OSATs like Amkor and ASE. While the current Groq LPU (LP30) is still using Flip chip packaging, we are expecting the next version (LP40 using TSMC N3) to migrate to CoWoS-R packaging. In addition, networking chips, especially those with CPO / NPO adoption, are an incremental driver for CoWoS demand due to increased networking bundle rates and much larger package sizes. Server CPU packaging, in particular, could be a good area for strong growth for OSATs, given the smaller package size (2-3.5x reticle limit) and limited complexity.
- **WMCM capacity expanding, non-Apple customers considering similar solutions in 2028:** Given stronger iPhone demand and higher indicative build rates for iPhone Pro/ Foldable production in 2H26 (see link), we have moved up our WMCM capacity forecasts and now expect 75/90k wfpm capacity by end 2027/28. Early discussions are now ongoing, in our view, with QCOM and Mediatek considering WMCM-like packaging methodologies for their flagship SoCs in 2028, based on our channel checks, given the rising demand for low-latency and wide bandwidth in SoC-DRAM communication for AI smartphones. For Apple, we see some likelihood of WMCM-like packaging technology adoption beyond iPhones, especially for Macbooks.

Note: Alphabet (GOOGL, OW), Amazon.com (AMZN, OW) and Meta Platforms (META, OW) are covered by Doug Anmuth. Advanced Micro Devices (AMD, N), Broadcom (AVGO, OW), Marvell Technology (MRVL, OW), Intel (INTC, UW) and NVIDIA (NVDA, OW) are covered by Harlan Sur. Amkor Technology (AMKR, OW) is covered by Peter K. Peng. Apple (AAPL, OW) is covered by Samik Chatterjee, CFA. Microsoft (MSFT, OW) is covered by Mark R. Murphy. Tesla (TSLA, UW) is covered by Ryan Brinkman.Open AI is covered by Brenda Duverce.

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Table 1: CoWoS allocation breakdown

						% Revision vs prior ests		
CoWoS Consumption by customer (k wafer per year)	**2023**	**2024**	**2025**	**2026E**	**2027E**	**2026E**	**2027E**	**JPM Comments**
NVIDIA	70	192	400	720	1120	*7%*	*12%*	Slight downtick in Rubin due to persistent HBM4 issues, Meaningful uptick in GB300. Overall 2026 number raised due to GB300, Spectrum X and Vera ramp. Uptick in 2027 demand indications due to Rubin, Rubin Ultra 2-die, Vera and Spectrum X. LPU40 will use CoWoS-R from 2028.
At TSMC	*70*	*127*	*385*	*680*	*995*	*5%*	*12%*	2026 CoWoS-L at TSMC, others at OSAT, 2027 Rubin Ultra assuming 2-die-on-interposer solution.
CoWoS-S / R	*70*	*97*	*30*	*5*	*0*			Vera CPU using CoWoS-R. Start with TSMC but will eventually migrate to OSATs from late 2026.
CoWoS-L	*0*	*30*	*355*	*675*	*995*	*5%*	*12%*	Majority of CoWoS to migrate to CoWoS-L by 2H25. Rubin Ultra likely to remain on CoWoS-L. Feynman likely to be still on CoWoS, given slower progress for CoPoS. Final decision end 2026
Outside TSMC (CoWoS-S/R)	*0*	*65*	*15*	*40*	*125*	*33%*	*14%*	Outsourcing ratio picking up in 2026 again as Vera outsourcing to Amkor starts to pick up more momentum in 2027, followed by ASE/SPIL. LPU40 could also be outsourced to OSATs in 2028
AMD	10	45	52	80	180	*4%*	*50%*	MI450 ramp in late 2026; moving to CoWoS-L for MI450 onwards; forecasts incl. Xilinx; Meaningful upside forecasts to 2027 due to MI400 and Venice CPU demand. Venice will move to ASE from 2027
CoWoS-S	10	45	52	25	10	*0%*	*NA*	MI350 and Xilinx main CoWoS-S customer. AMD also has non-AI projects migrating to 2.5D packaging in 2H26. Likely to be mostly at ASE. Not captured in these forecasts
CoWoS-L	0	0	0	55	170	*6%*	*42%*	CoWoS-L move likely only for MI400 family and beyond, Venice CPUs also to use CoWoS-L.
Broadcom	40	70	96	250	425	*0%*	*6%*	TPU v7 (Ironwood) and v8ax most of the volume in 2026 and 2027, with small volume for v9 in late 2027. MTIA CoWoS ramp seems slower, OpenAI in 2027. Tomahawk 6 also using CoWoS-S.
CoWoS-S at TSMC	40	70	91	220	260	*0%*	*18%*	CoWoS-S is still mainstream in 2026, but more adoption of CoWoS-L from 2027 for Meta, OpenAI and TPUv9 in late 2027
CoWoS-S outside TSMC	0	0	5	10	70	*0%*	*-30%*	Outsourcing starting to pick up - Trialling ASE and Amkor for Networking projects in 2027. OSAT qualification slower than expected
CoWoS-L	0	0	0	20	95	*0%*	*19%*	Starting to use CoWoS-L for some projects including advanced TPU models; also likely to incorporate SoIC for some advanced ASICs for TPUv9, MTIA and OpenAI Titan2 in 2027/28.
Alchip + AWS	7	14	5	65	165	*0%*	*6%*	Trn2 upside in 1H26, Trn3 ramp in mid 2026, upside to lifetime volumes for Trn3. Most Trn3 CoWoS allocation through AWS or Alchip. Small overflow to other customers due to excess demand
Marvell (incl AWS for Trn2)	2	13	75	35	30	*0%*	*-25%*	Near-term upside to Trn2. Not seeing much Trn3 CoWoS or OSAT allocation. MSFT MAIA 3 to ramp in 2027. Not seeing a big ramp for other CoWoS projects in 2027.
MediaTek	0	0	0	30	125	*67%*	*108%*	2026 TPUv8x volume strengthening in 2026/27. TPUv9 Humufish - Plan A on Intel EMIB and Plan B on CoWoS-L
Others	5	16	24	35	50	*-22%*	*-33%*	Includes Cisco, Microsoft, GUC, Socionext, other ASIC design houses and smaller startup customers etc.; some non-AI chips also using CoWoS (networking chips for various vendors, some small volume server CPUs etc.).
Overall Total CoWoS Consumption	**134**	**350**	**652**	**1,215**	**2,095**	***4%***	***13%***	
yoy		*161%*	*86%*	*86%*	*72%*			
CoWoS Consumption by customer (k wafer per year)	**2023**	**2024**	**2025**	**2026E**	**2027E**	**2026E**	**2027E**	**JPM Comments**
Total TSMC	**134**	**290**	**592**	**1,145**	**1,815**	***2%***	***11%***	TSMC includes sub-contracting of oS to ASE/SPIL from 2025 and sub-contracting of Interposer to Vanguard
Total Others (OSATs)	0	60	60	70	280	*56%*	*27%*	Mainly ASE/SPIL and Amkor, non-TSMC utilization uneven in 2025, given move to CoWoS-L; more full-stack CoWoS from 2H26. Intel EMIB not modeled here, but main volume ramp only in 2028.
Overall Total CoWoS Consumption	**134**	**350**	**652**	**1215**	**2095**	***4%***	***13%***	

Source: Company data, J.P. Morgan estimates. Note: Capacity allocation is before adjusting for yield losses, which may vary by accelerator and package type.

Table 2: WMCM forecasts

WMCM Consumption (K wafer per year)	**2023**	**2024**	**2025**	**2026E**	**2027E**	**JPM Comments**
Apple	0	0	0	417	720	All high-end iPhone 18 models in 2H26E using WMCM.
Number of iPhones (M units)				88	151	Likely to adopt for A20 Pro based models on N2. Encompassing iPhone foldable, Pro and Pro max.
Utilization				100%	100%	
Gross Die per wafer				210	210	Expect Package size to be 50% larger than InFO with ~200 dies per Wafer due to side by side stacking of LPDDR5.
% Yield				98%	98%	
TSMC WMCM Capacity (k wafer per year)				**426**	**735**	

Source: Company data, J.P. Morgan estimates.

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Table 3: GPU and AI accelerators chip-level shipment forecasts

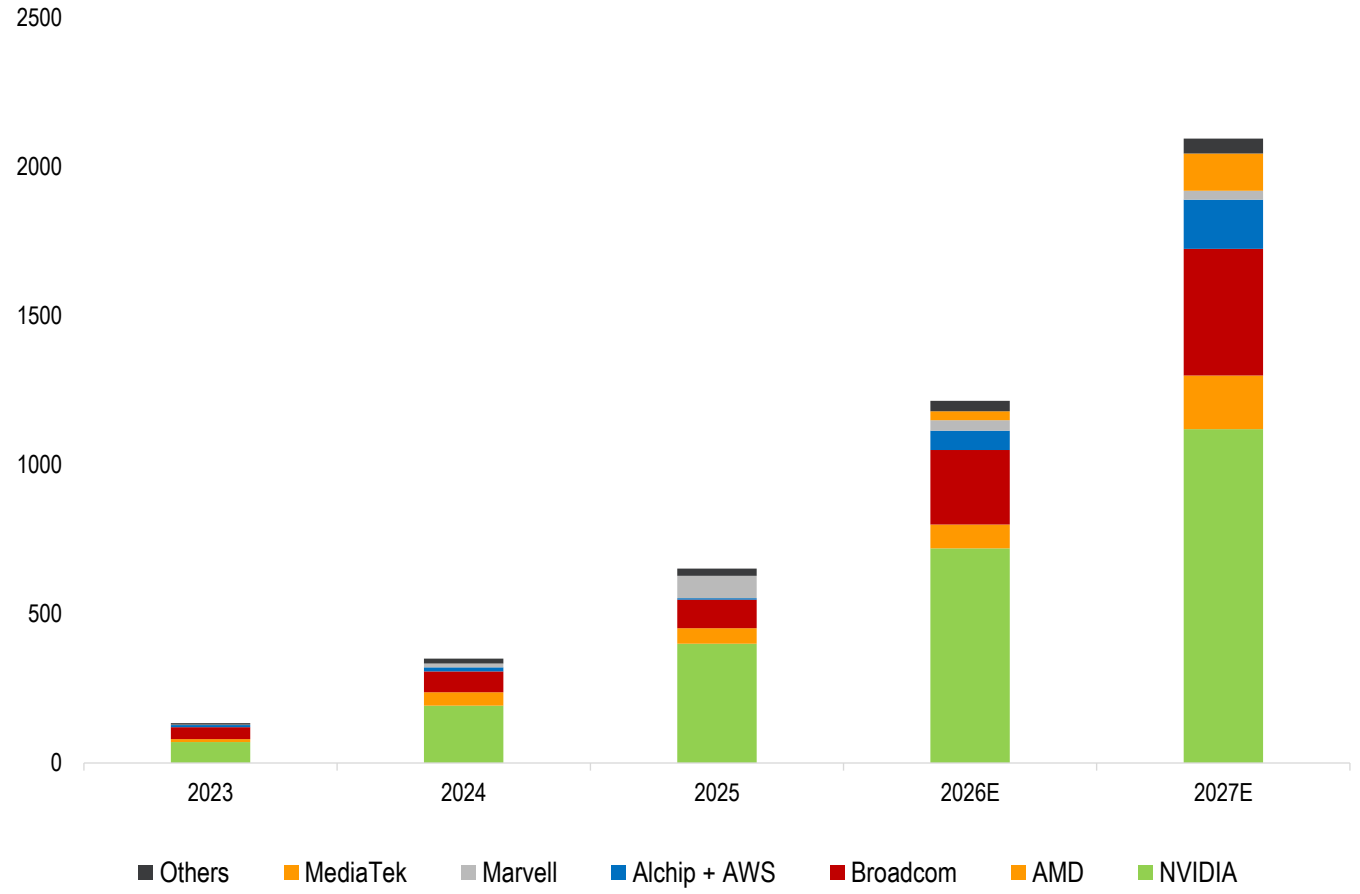
GPU and Accelerator Units (M)	2023	2024	2025	2026E	2027E
NVDA					
Hopper Series	1.7	4.3	1.0	0.4	-
Blackwell Series	-	0.2	5.2	6.4	1.0
Rubin Series	-	-	-	2.1	7.3
Rubin Ultra Series (2 die equivalent)	-	-	-	-	1.6
Total NVDA GPU Units	**1.7**	**4.5**	**6.2**	**8.9**	**9.9**
NVDA eq GPU die units	*1.7*	*4.7*	*11.4*	*17.4*	*23.0*
Vera CPU	-	-	-	0.6	3.0
Others Including Spectrum X	-	-	-	0.2	0.4
AMD					
MI300/325	0.1	0.5	0.4	-	-
MI350	-	-	0.3	0.2	-
MI450	-	-	-	0.4	1.0
Total AMD GPU Units	**0.1**	**0.5**	**0.7**	**0.6**	**1.0**
Google TPUs					
v4	0.7	0.4	-	-	-
v5	0.5	1.3	-	-	-
v6 /v7 (Trillium/Ironwood)	-	-	1.7	2.7	1.7
v8t - Zebrafish - Mediatek	-	-	-	0.6	2.5
v8i - Sunfish - Broadcom	-	-	0.1	1.2	3.8
v9 - Pumafish - Broadcom	-	-	-	-	0.1
v9 - Humufish - Mediatek				-	-
Total TPU Units	**1.2**	**1.7**	**1.8**	**4.5**	**8.0**
AWS					
Inferentia 2	0.3	0.5	0.1	-	-
Trainium 2	-	0.3	1.5	0.6	-
Trainium 3	-	-	-	1.3	3.3
Total Inferentia / Trainium Units	**0.3**	**0.8**	**1.5**	**1.9**	**3.3**
Meta					
MTIA v2T (Athena)				0.3	0.2
MTIA v3 (Iris)				-	0.4
Total MTIA units (with CoWoS)				**0.3**	**0.5**
Microsoft					
MAIA 200 - GUC				0.1	0.1
MAIA 300 - Marvell				0.1	0.6
Total MAIA units				**0.2**	**0.7**

Source: Company data, J.P. Morgan estimates.

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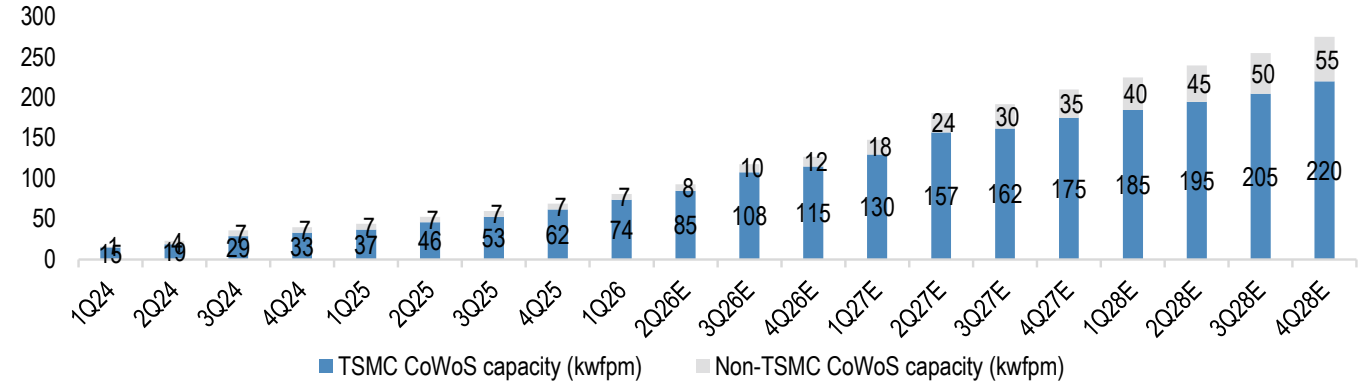
Figure 1: Customer mix for CoWoS

k wafers per year



Source: Company data, J.P. Morgan estimates.

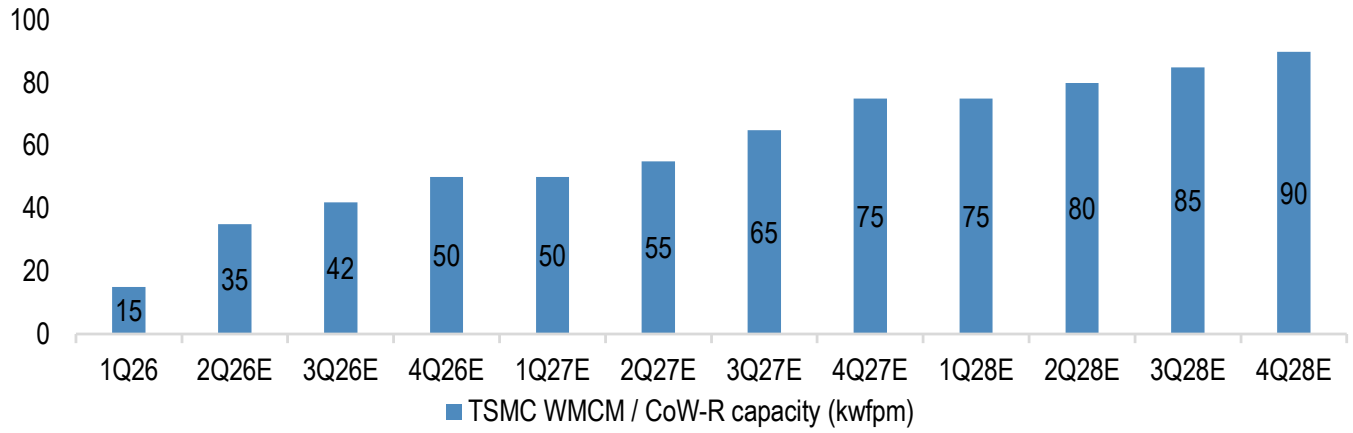
Figure 2: CoWoS capacity – TSMC/non-TSMC



Source: Company data, J.P. Morgan estimates.

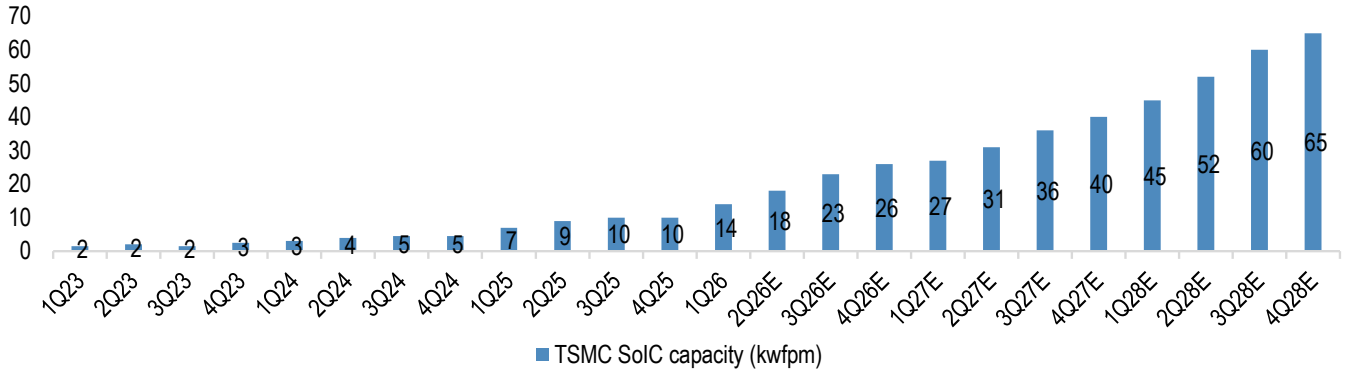
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Figure 3: WMCM/CoW-R capacity – TSMC



Source: J.P. Morgan estimates.

Figure 4: SoIC capacity – TSMC



Source: Company data, J.P. Morgan estimates.

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Table 4: Glossary of important terms

HBM	High Bandwidth Memory	HBM is a high-speed computer memory interface for 3D-stacked synchronous dynamic random-access memory (SDRAM) from Samsung, Micron and SK Hynix.
CoWoS	Chips-on-Wafer-on-Substrate	TSMC's 2.5D interposer-based packaging technology for high-performance computing applications.
CoWoS - S	Chips-on-Wafer-on-Substrate with Silicon Interposer	A CoWoS technique using silicon interposer as the bridge between chip and substrate.
CoWoS - R	Chips-on-Wafer-on-Substrate with Redistribution Layer Interposer	A CoWoS technique using redistribution layer interposer (RDL) to replace silicon interposer, enabling higher packaging size flexibility and lower cost.
CoWoS - L	Chips-on-Wafer-on-Substrate with Local Silicon Interconnect	A CoWoS technique using local silicon interconnect (LSI) to connect dies at high speed rate, while the other area on the chip will use RDL.
COW - R	Chip-on-Wafer with Redistribution Layer Interposer	The first part of the CoWoS process, where the logic chip and HBMs are attached to the RDL interposer.
RDL	Redistribution Layer	A layer of metal interconnects that redistributes I/O access across the chip, facilitating flexible and efficient chip-to-chip connections, particularly in advanced packaging techniques like 2.5D and 3D integration.
WMCM	Wafer-level Multichip Module	An approach that integrates multiple chips (CPU, GPU, memory, etc.) at the wafer stage before slicing them into individual modules. Unlike traditional InFO (Integrated Fan-Out) packaging, focusing on single-die integration, WMCM enables more flexibility in combining different components while maintaining a small footprint.
XPU	X processing unit	The "X" in "XPU" stands for any compute architecture (CPU, GPU, ASIC etc.) that is suitable for different applications.
TPU	Tensor processing unit	Google Cloud TPUs are cusomized AI accelerators, optimized for training and inference of AI models.
LPDDR	Low Power Double Data Rate	Also known as LPDRAM, LPDDR is used in devices requiring speedy, high-bandwidth data rates without compromising power efficiency.
CPO	Co-Packaged Optics	An integration of optical componnents and ASICs on a single packaged substrate, enabling high-speed data transmission and less power loss.
ASIC	Application-Specific Integrated Circuit	ASICs (application-specific integrated circuits) are customized chips for certain special purposes, and right-of-use is limited to the chip designer only.
CSP	Cloud Service Provider	A third-party company that provides a cloud-based platform for businesses to access on demand over a network, including compute, storage, and infrastructure services.
FOCoS	Fan Out Chip on Substrate (similar to TSMC's CoWoS)	A fan-out package flip-chip placed on a high pin count ball grid array (BGA) substrate. The fan-out package has an RDL allowing the construction of shorter die-to-die (D2D) interconnections between chips.
Trn	Trainium	Trainium are chips developed by AWS specifically for AI training and inference, which deliver high performance while saving costs.
InFO	Integrated Fan-Out	A wafer-level integration technology features high-density RDL and Through InFO Via (TIV) for enhanced interconnect performance. It supports various 2D and 3D package schemes optimized for mobile and high-performance computing applications.
EIC-PIC	Electronic/Photonic Integrated Circuit	EICs utilize electronic components (transistors, capacitors) for electrical signal processing, while PICs use optical components (waveguides, lasers) for light manipulation in data transmission. EICs handle electrons, and PICs handle photons.
CoPoS	Chip-on-Panel-on-Substrate	TSMC's CoPoS is a rectangular substrate evolution of CoWoS, offering more usable space than traditional round wafers, enhancing output efficiency and reducing costs.
EMIB	Embedded Multi-die Interconnect Bridge	Intel's EMIB is an advanced packaging technology that embeds silicon bridges into an organic substrate. It enables multiple chiplets to communicate side-by-side with high bandwidth and low latency, without the need for full-size silicon interposers.

Source: J.P. Morgan.

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Investment Thesis, Valuation and Risks

TSMC *(Overweight; Price Target: NT$2500.0)*

Investment Thesis
We expect TSMC's structural growth drivers to remain very strong as leading-edge supply (N4, N3, and N2) stays tight well into 2027 or early 2028, given accelerating AI demand, continued growth in N3, N2 and advanced back-end revenues, and long lead time for capacity build despite accelerated capex. We believe the set-up for TSMC stock looks quite favorable in the next few quarters, with potential upside to its long-term capex targets, 2026 revenue guidance, and GMs beating due to high UTR and ASP uptick. Given industry-wide shortage, we expect competitive noise to persist, but achieving technology and manufacturing milestones and winning customer acceptance would be the key challenge for the chasing pack, given TSMC tech and execution leadership and 3-5 year window for design and manufacturing ramp.

Valuation
Our Dec-26 PT of NT$2,500 is based on ~20x 12-month forward P/E and reflects better GMs and slightly faster growth. Our target multiple is higher than TSMC's five-year average historical multiple.

Risks to Rating and Price Target
Key downside risks to our rating and price target include: (1) the debate on the duration of the AI capex growth cycle and (2) any negative impact from weak PC/Smartphone demand in 2H26.

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TSMC (2330.TW, 2330 TT) Price Chart



Date	Rating	Price (NT$)	Price Target (NT$)
20-Oct-23	OW	546.0	700
04-Jan-24	OW	578.0	750
19-Jan-24	OW	588.0	770
06-Mar-24	OW	730.0	850
07-Apr-24	OW	780.0	900
17-Jun-24	OW	922.0	1,080
19-Jul-24	OW	1005.0	1,200
18-Oct-24	OW	1035.0	1,500
13-Apr-25	OW	889.0	1,300
18-Apr-25	OW	847.0	1,275
24-Sep-25	OW	1340.0	1,550
17-Oct-25	OW	1485.0	1,700
07-Jan-26	OW	1705.0	2,100
16-Jan-26	OW	1690.0	2,250
02-Apr-26	OW	1855.0	2,400
17-Apr-26	OW	2085.0	2,500

Source: Bloomberg Finance L.P. and J.P. Morgan; price data adjusted for stock splits and dividends.
Initiated coverage Apr 28, 2002. All share prices are as of market close on the previous business day.

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